

UMA & Optimus Schematics Document

Sandy Bridge

Intel PCH

2010-10-27

REV : -1

DY :None Installed
UMA:UMA platform installed
OPS:Optimus

55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A3

Document Number

LA470

Rev

-1

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##OnMainBoard

55.4KZ01.S18G S19G

Title			
Block Diagram			
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SSID = CPU

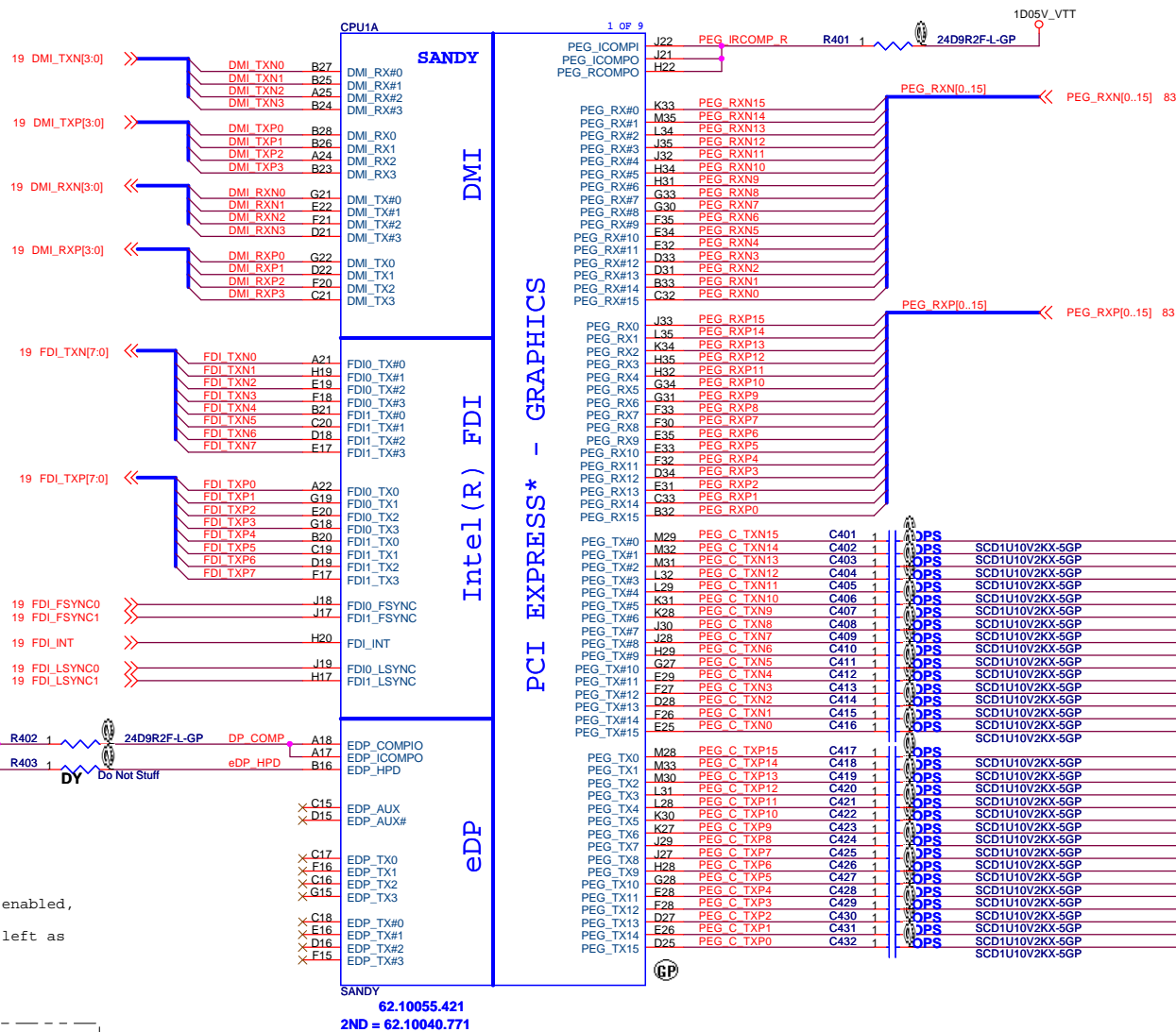
Note:
EDP_ICOMPO and EDP_COMPIO should not be left floating.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

If HPD is disabled while eDP interface is still enabled, connect it to CPU VCCIO via a 10-k ohm pull-up resistor on the motherboard. This signal can be left as no connect if entire eDP interface is disabled.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

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55.4KZ01.S18G S19G

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Title

CPU (PCIe/DMI/FDI)

Size A3

Document Number

Rev

Date

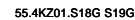
Thursday, November 04, 2010

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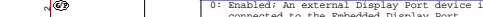
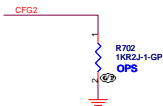
CPU (DDR)

Rev

-1

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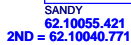
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Display Port Presence Strap	
CFG4	1: Disabled: No Physical Display Port attached to Embedded Display Port
	0: Enabled: An external Display Port device is connected to the Embedded Display Port

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

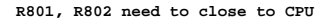
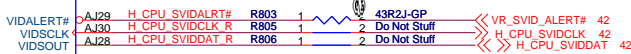
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SANDY

CORE SUPPLY

SENSE LINES

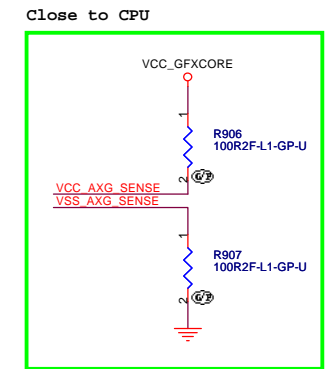


緯創資通

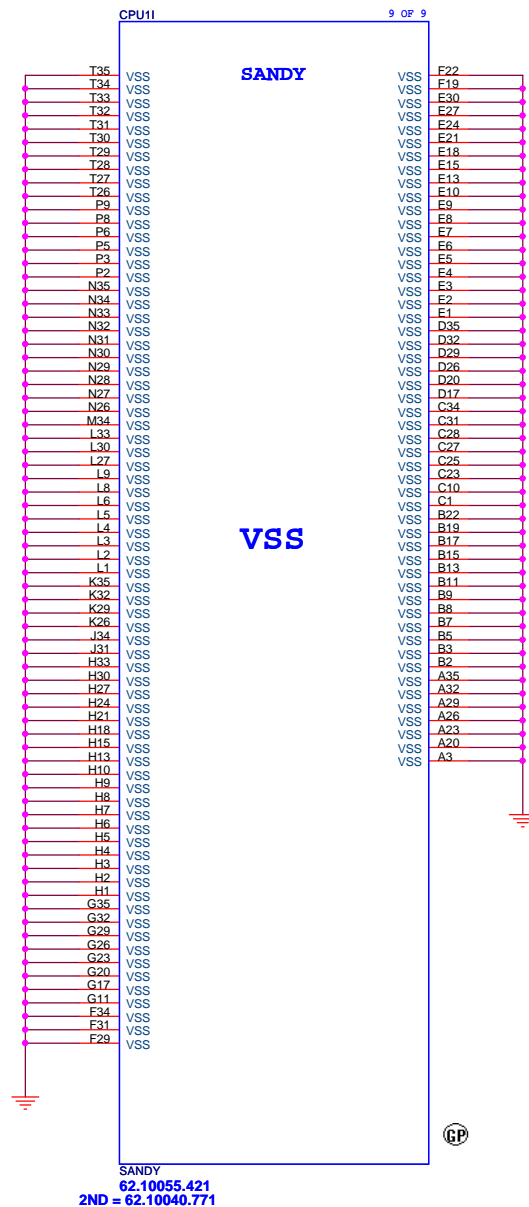
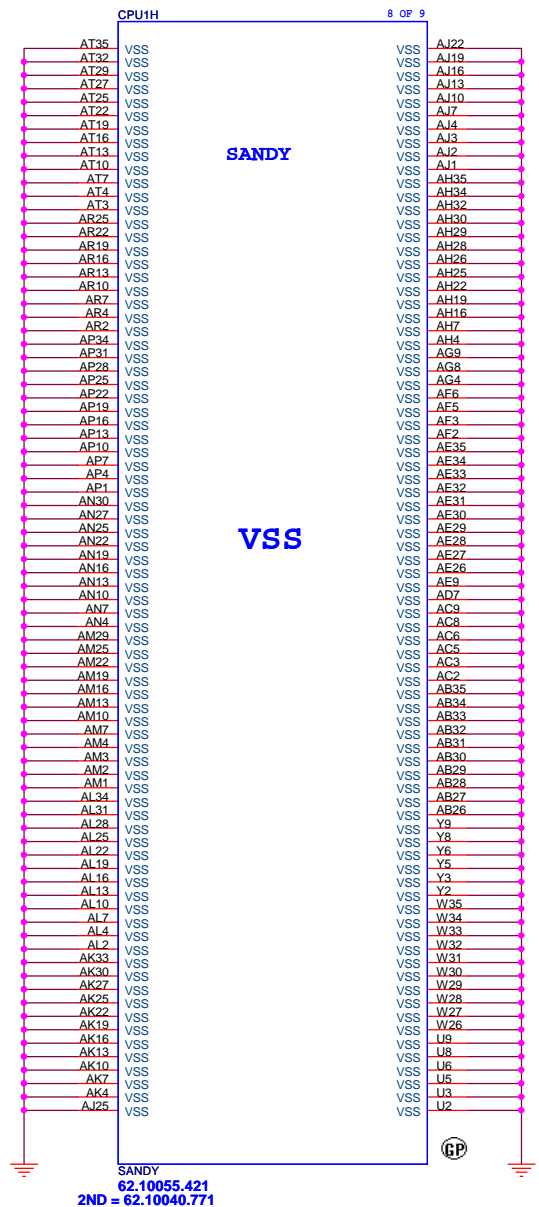
Title	CPU (VCC CORE)
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SSID = CPU



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Title CPU (VSS)

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5	4	3	2	1
D				
C				
B				
A				

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XDP			
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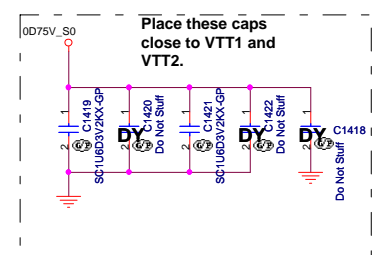
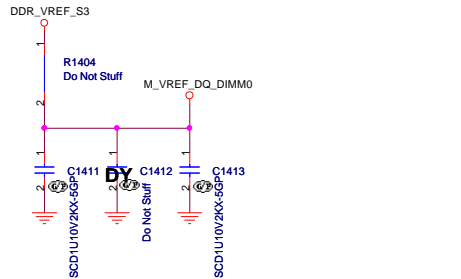
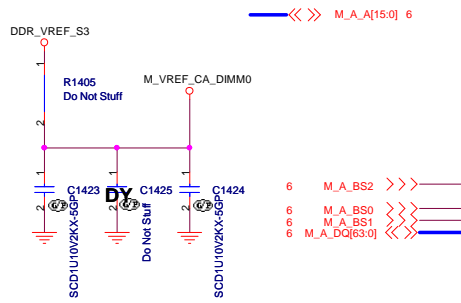
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Size <div>A4</div>	Document Number <div>LA470</div>	Rev <div>-1</div>
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SSID = MEMORY



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M_A_DQS#[7:0] 6

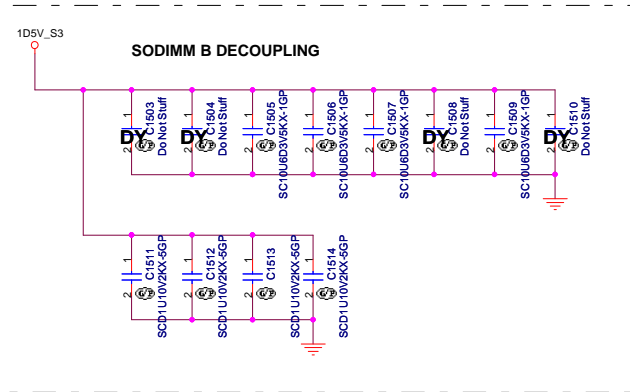
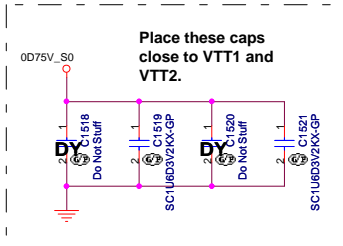
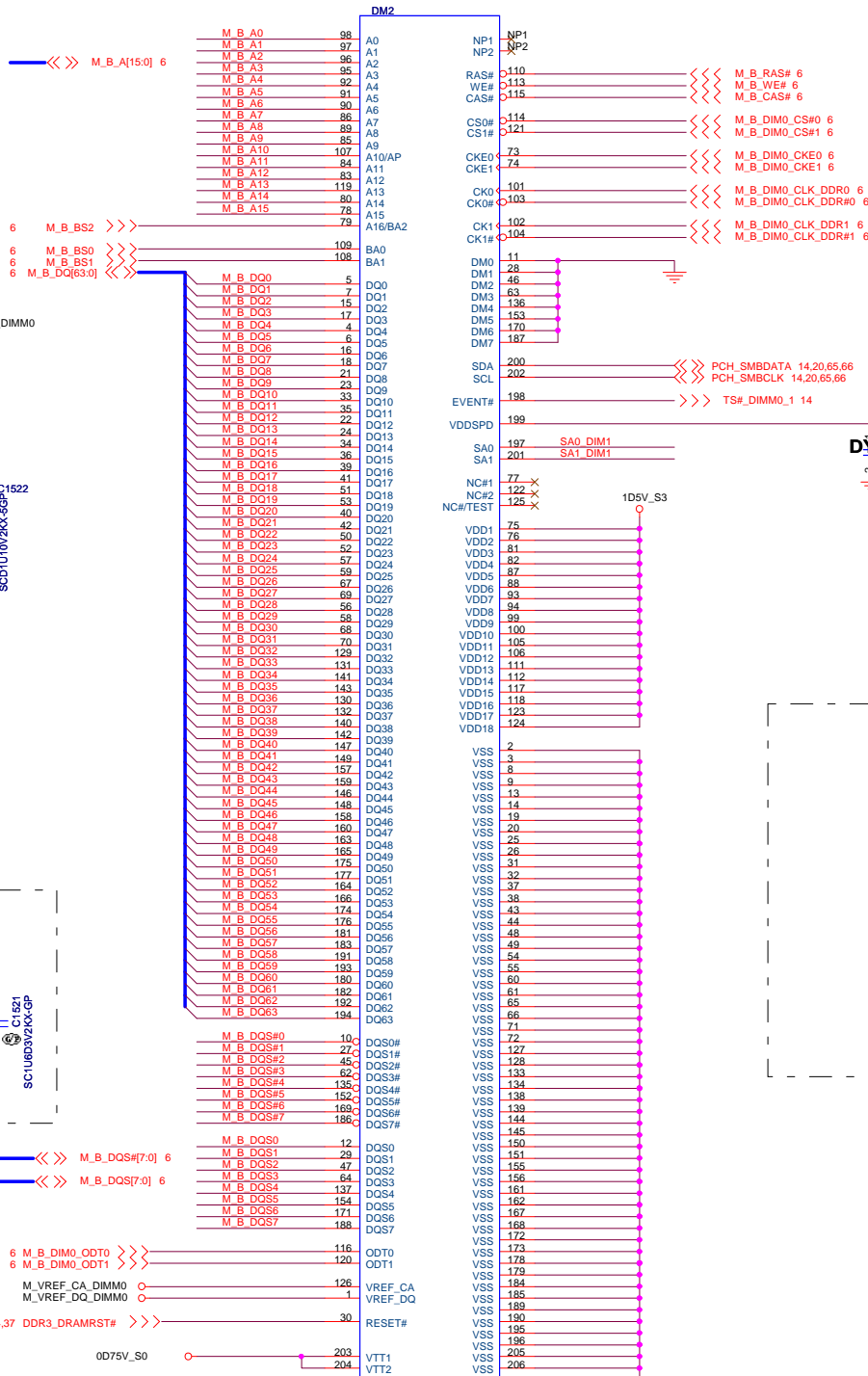
6 M_A_DIMM0_ODT0
6 M_A_DIMM0_ODT1

15,37 DDR3_DRAMRST#

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M_A A1	97	M_A DQ1	7	M_A DQS#1	105
M_A A2	96	M_A DQ2	15	M_A DQS#2	106
M_A A3	95	M_A DQ3	17	M_A DQS#3	107
M_A A4	94	M_A DQ4	4	M_A DQS#4	108
M_A A5	93	M_A DQ5	6	M_A DQS#5	109
M_A A6	92	M_A DQ6	16	M_A DQS#6	110
M_A A7	91	M_A DQ7	18	M_A DQS#7	111
M_A A8	90	M_A DQ8	21	M_A DQS#0	112
M_A A9	89	M_A DQ9	23	M_A DQS#1	113
M_A A10	88	M_A DQ10	33	M_A DQS#2	114
M_A A11	87	M_A DQ11	35	M_A DQS#3	115
M_A A12	86	M_A DQ12	22	M_A DQS#4	116
M_A A13	85	M_A DQ13	24	M_A DQS#5	117
M_A A14	84	M_A DQ14	34	M_A DQS#6	118
M_A A15	83	M_A DQ15	36	M_A DQS#7	119
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		M_A DQS#7	255		

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CKE0	CKE1		
CK0	CK0#		
CK1	CK1#		
DM0	DM1	DM2	DM3
DM4	DM5	DM6	DM7
SDA	SCL		
EVENT#			
VDDSPD			
SA0	SA1	SA0_DIM0	SA1_DIM0
NC#1	NC#2		
NC#/TEST			1D5V_S3
VDD1	VDD2	VDD3	VDD4
VDD5	VDD6	VDD7	VDD8
VDD9	VDD10	VDD11	VDD12
VDD13	VDD14	VDD15	VDD16
VDD17	VDD18		
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VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS
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VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS
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VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS

SSID = MEMORY



55.4KZ01.S18G S19G

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Title			DDR3-SODIMM2
Size			Document Number
Custom			LA470
Date:			Thursday, November 04, 2010
Sheet			15 of 103
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(Blanking)

55.4KZ01.S18G S19G

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

DDR3-SODIMM2

Size
A4

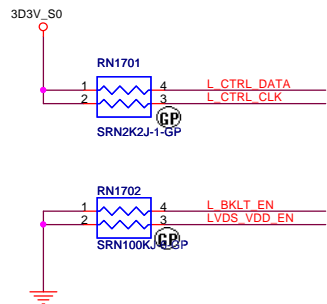
Document Number

LA470

Rev
-1

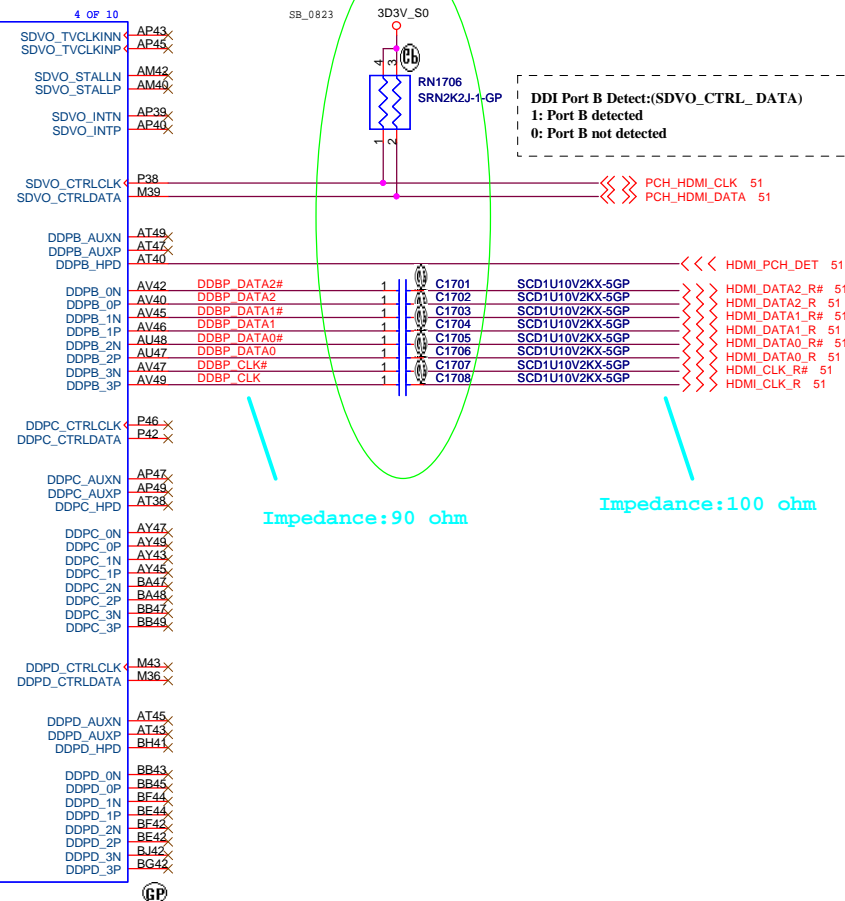
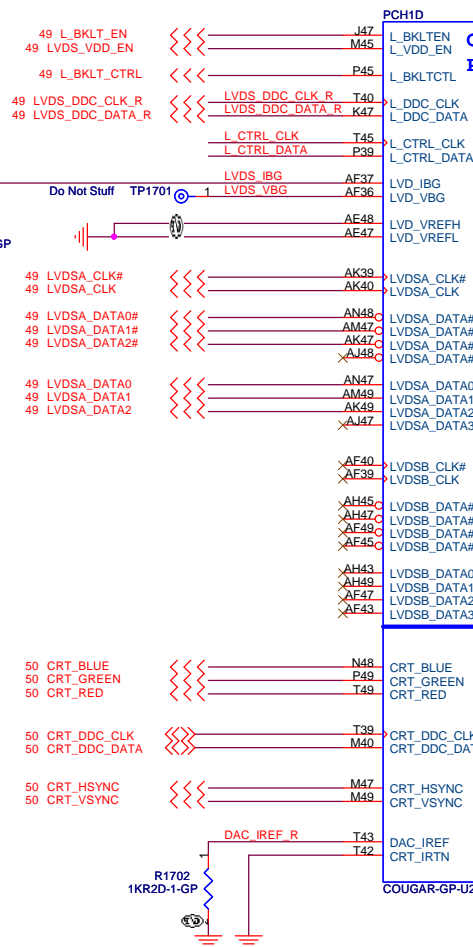
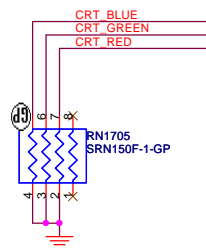
Date: Thursday, November 04, 2010

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Place near PCH

Close to PCH side



Impedance:90 ohm

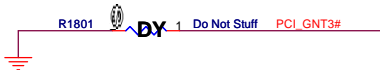
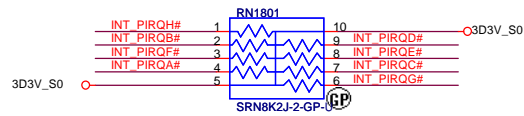
Impedance:100 ohm

55.4K201.S18G S19G

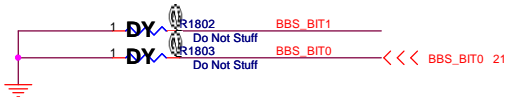
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			PCH (LVDS/CRT/DDI)	
Size	Document Number	Rev		
A3	LA470	-1		
Date:	Thursday, November 04, 2010	Sheet	17	of 103

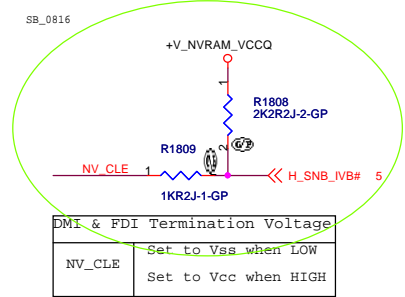
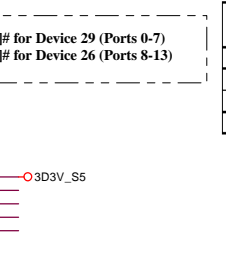
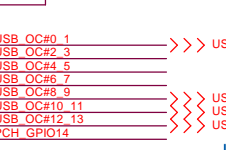
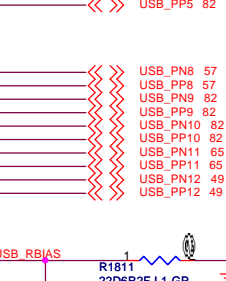
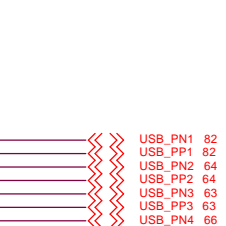
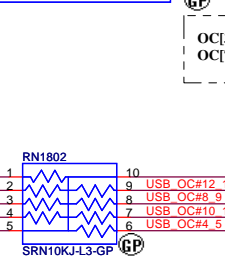
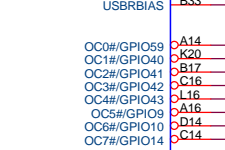
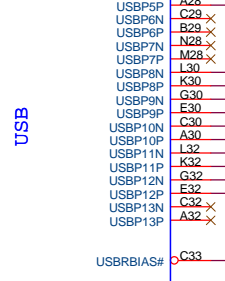
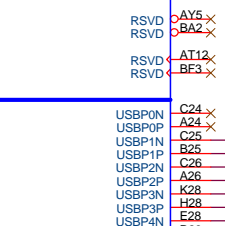
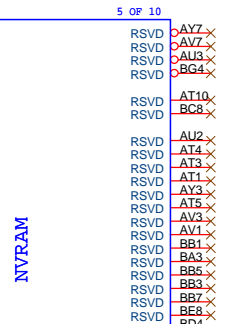
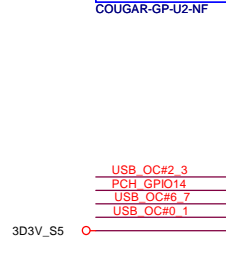
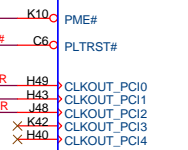
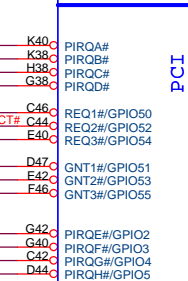
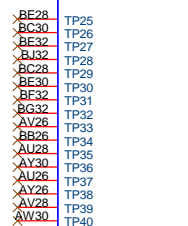
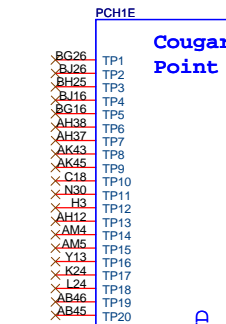
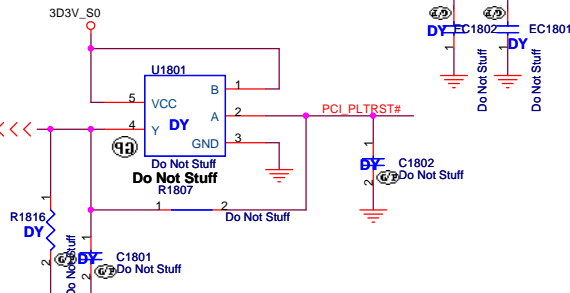
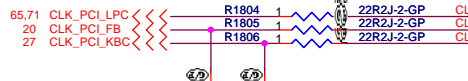
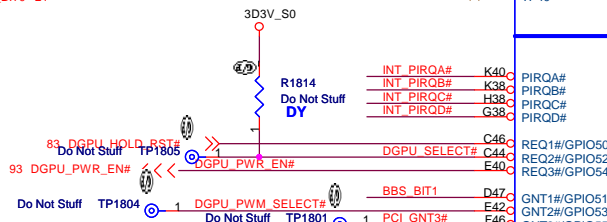
SSID = PCH



A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default



BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)



DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

USB Table

Pair	Device
0	X
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA / USB CHARGE
9	USB Ext. port 2
10	USB Ext. port 3
11	Mini Card1 (WLAN)
12	CAMERA
13	X

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

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Title		PCH (PCI/USB/NVRAM)	
Size	Document Number	Rev	-1
A3	LA470		
Date	Thursday, November 04, 2010	Sheet	18 of 103

SSID = PCH

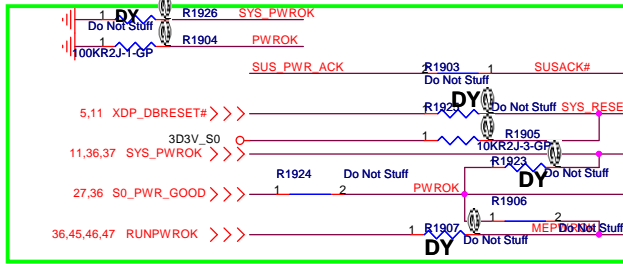
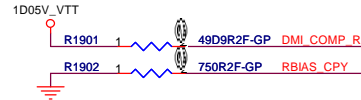
4 DMI_RXN[3:0] <<<<
4 DMI_RXP[3:0] <<<<
4 DMI_TXN[3:0] <<<<
4 DMI_TXP[3:0] <<<<

FDI_TXN[7:0] 4
FDI_TXP[7:0] 4

Deep S4/S5 Supported

Deep S4/S5 Not Supported

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.



PCH1C

Cougar Point

DMI
FDI

System Power Management

COUGAR-GP-U2-NF

3 OF 10

FDI_RXN0 FDI_RXN1 FDI_RXN2 FDI_RXN3 FDI_RXN4 FDI_RXN5 FDI_RXN6 FDI_RXN7
FDI_TXN0 FDI_TXN1 FDI_TXN2 FDI_TXN3 FDI_TXN4 FDI_TXN5 FDI_TXN6 FDI_TXN7
FDI_RXP0 FDI_RXP1 FDI_RXP2 FDI_RXP3 FDI_RXP4 FDI_RXP5 FDI_RXP6 FDI_RXP7
FDI_TXN0 FDI_TXN1 FDI_TXN2 FDI_TXN3 FDI_TXN4 FDI_TXN5 FDI_TXN6 FDI_TXN7
FDI_TXP0 FDI_TXP1 FDI_TXP2 FDI_TXP3 FDI_TXP4 FDI_TXP5 FDI_TXP6 FDI_TXP7

FDI_INT AW16 >>> FDI_INT 4
FDI_FSYNC0 AV12 >>> FDI_FSYNC0 4
FDI_FSYNC1 BC10 >>> FDI_FSYNC1 4
FDI_LSYNC0 AV14 >>> FDI_LSYNC0 4
FDI_LSYNC1 BB10 >>> FDI_LSYNC1 4

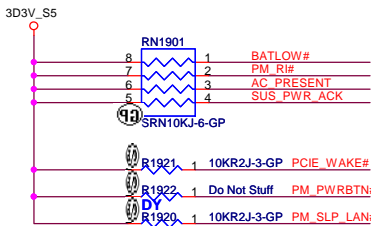
DSWVRMEN A18 DSWODVREN R1910 Do Not Stuff PM_RSMRST# RTC_AUX_S5
DPWROK E22 PCH_DPWROK DY R1911 Do Not Stuff
WAKE# B9 <<< PCIE_WAKE# 31,65,66
CLKRUN#/GPIO32 N3 <<< PM_CLKRUN# 27
SUS_STAT#/GPIO61 G8 PM_SUS_STAT# 1 TP1901 Do Not Stuff
SUSCLK#/GPIO62 N14 SUS_CLK R1913 Do Not Stuff >>> PCH_SUSCLK_KBC 27
SLP_S5#/GPIO63 D10 PM_SLP_S5# 1 TP1902 Do Not Stuff R1914 Do Not Stuff >>> PM_SLP_S4# 27,46
SLP_S4# H4 SLP_S4#_R R1915 Do Not Stuff >>> PM_SLP_S3# 27,36,37,47,92
SLP_S3# F4 SLP_S3#_R TP1903 Do Not Stuff
SLP_A# G10 PM_SLP_A# 1 TP1904 Do Not Stuff
SLP_SUS# G16 PM_SLP_SUS# 1 TP1904 Do Not Stuff
PMSYNCH AP14 H_PM_SYNC <<< H_PM_SYNC 5
SLP_LAN#/GPIO29 K14 PM_SLP_LAN# 1 TP1905 Do Not Stuff

SLP_S3# R 1 TP1906 Do Not Stuff

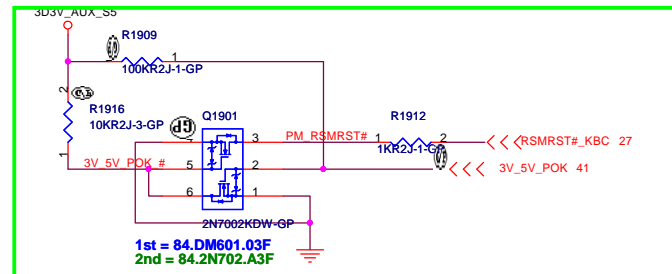
VccDSW3_3
DPWROK
VccSUS3_3
RSMRST#

- For platforms not supporting Deep S4/S5
- 1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
 - 2.DPWROK and RSMRST# will rise at the same time (connected on board)
 - 3.SLP_SUS# and SUSACK# are left as 'no connect'
 - 4.SUSWARN# used as SUSPWRDNACK/GPIO30

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled



This signal has an internal pull-up resistor

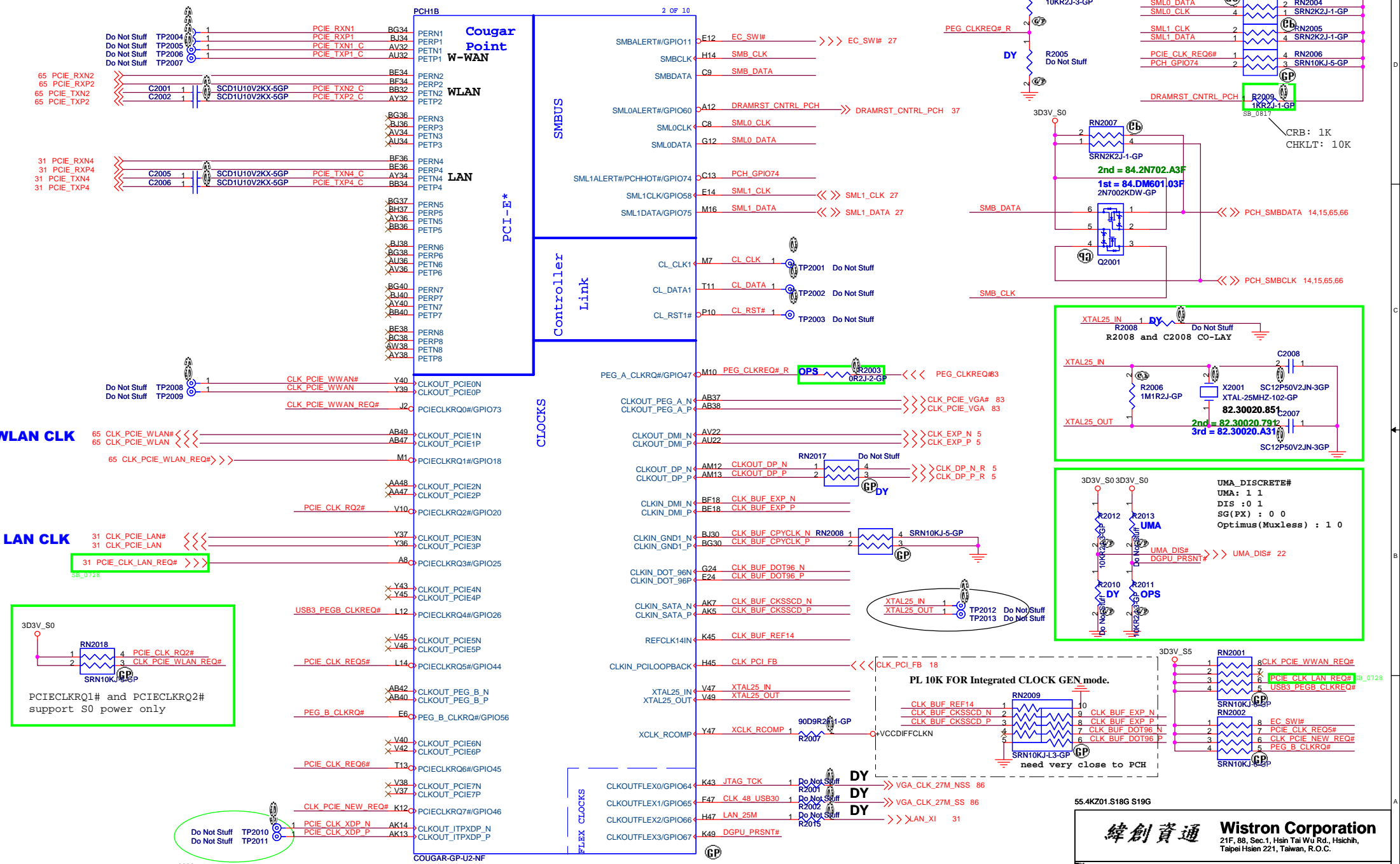


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Title		
PCH (DM I/FDI/PM)		
Size A3	Document Number	Rev
	LA470	-1
Date: Thursday, November 04, 2010	Sheet 19	of 103

SSID = PCH



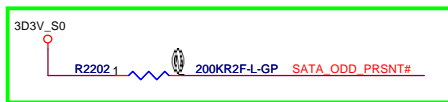
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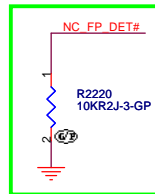
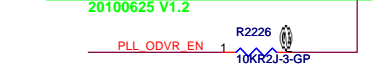
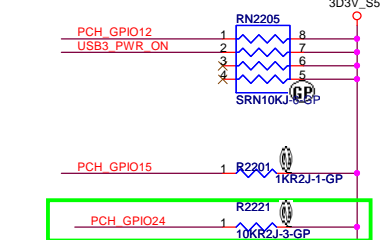
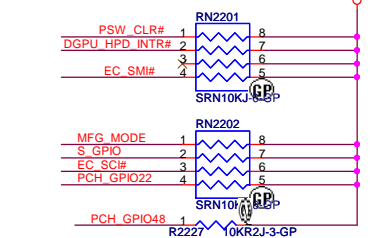
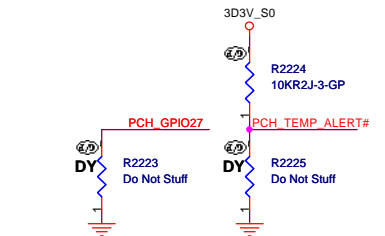
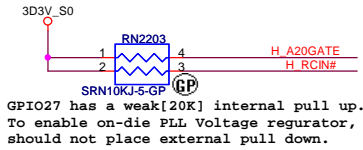
SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218

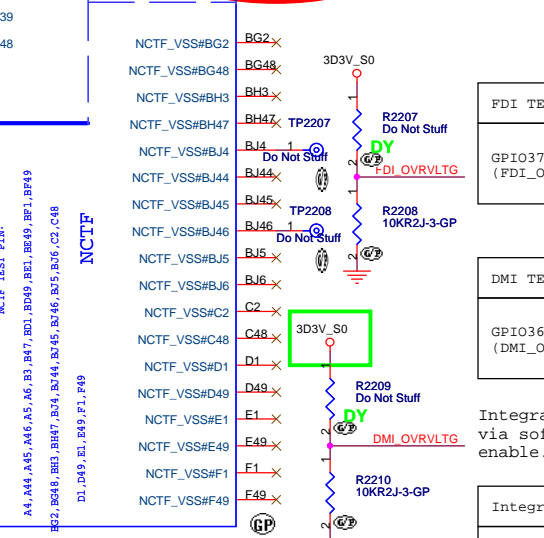
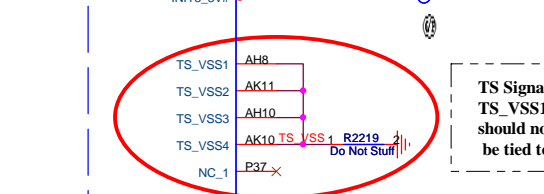
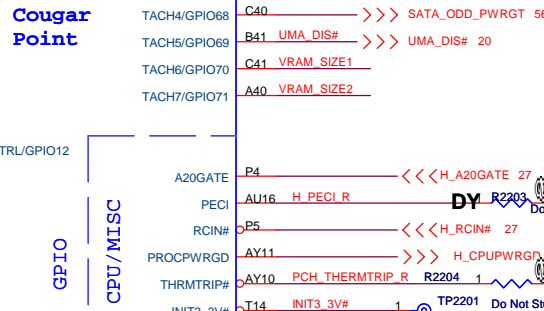
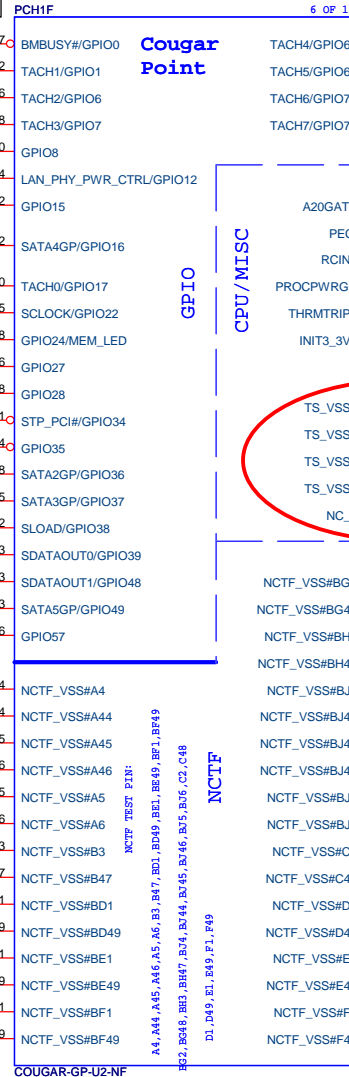
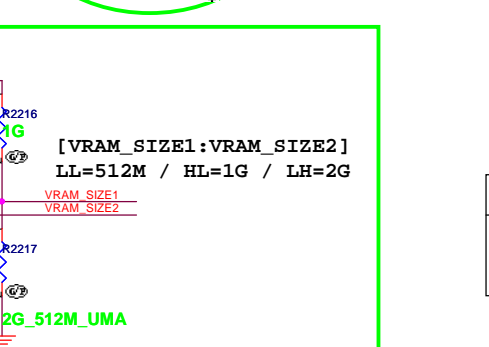
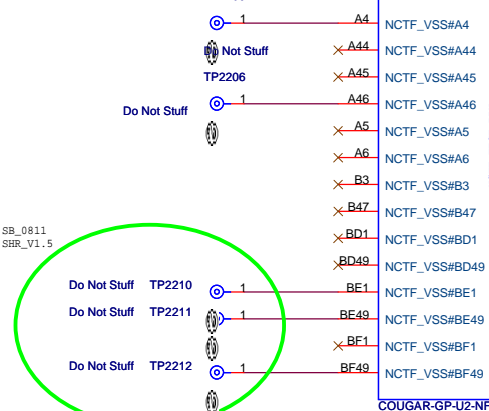
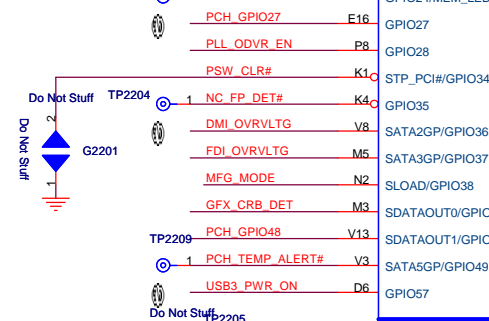
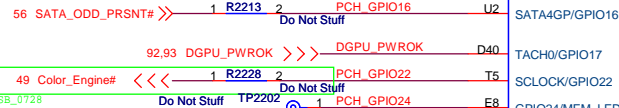
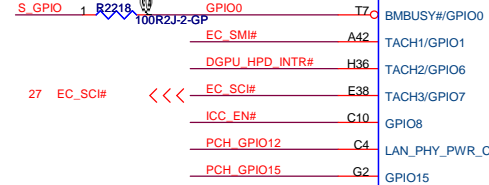
	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY



20100625 V1.2



20100705



TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved
via soft-strap. The default is integrated clock
enable.

55.4KZ01.S18G S19G

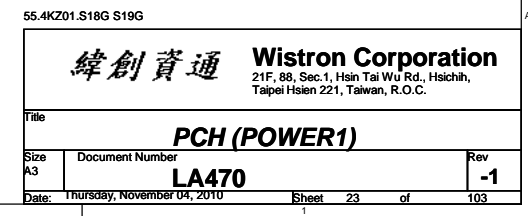
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Title			
PCH (GPIO/CPU)			
Size A3	Document Number		Rev
	LA470		-1
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PLL ON DIE VR ENABLE
NOTE: This signal has a weak internal pull-up 20K
ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT
DISABLED -- LOW (R2212 STUFFED)

PLL_ODVR_EN DY 1 R2212 Do Not Stru

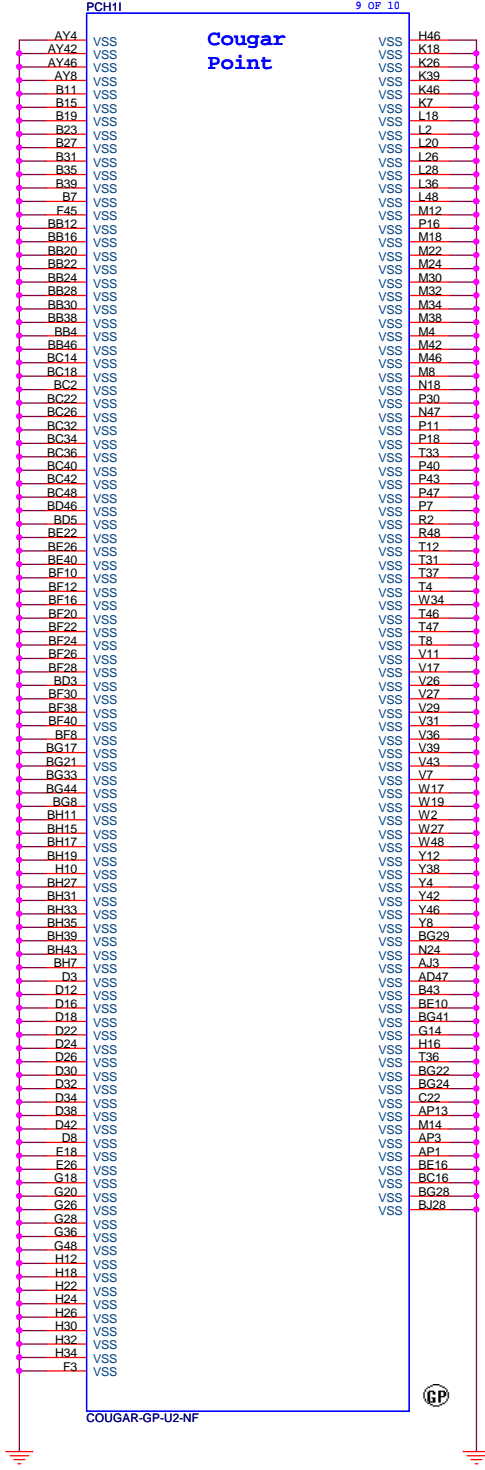
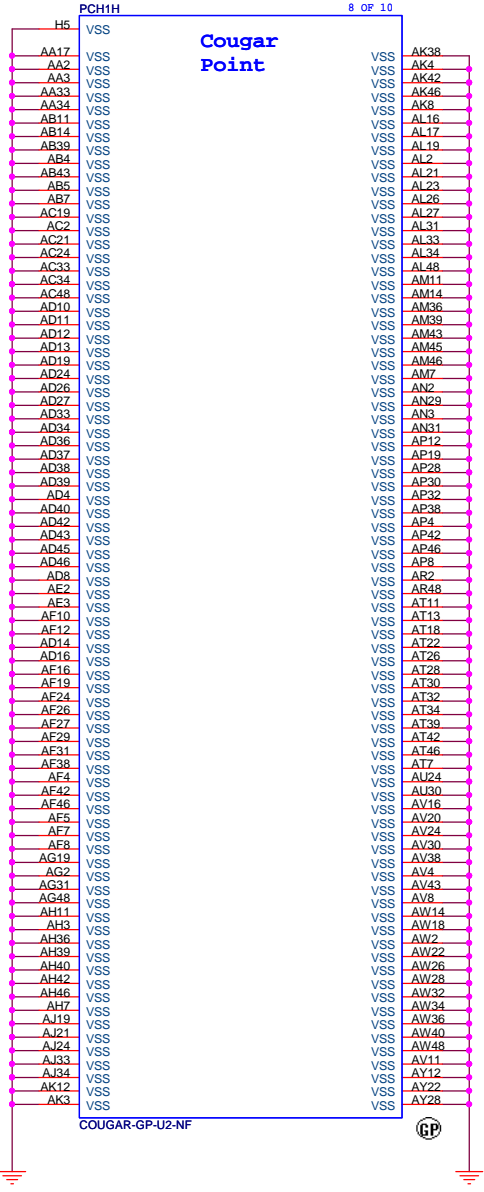
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SSID = PCH



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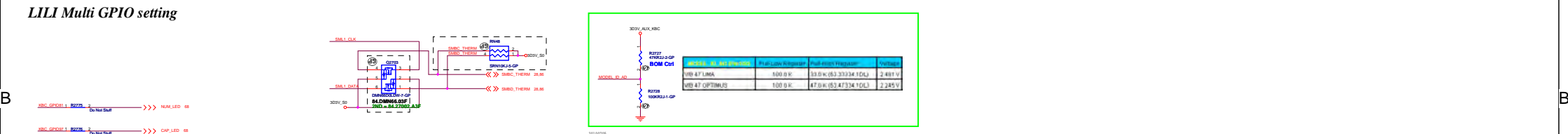
Title: **PCH (VSS)**

Size: A3	Document Number: LA470	Rev: -1
Date: Thursday, November 04, 2010	Sheet: 25	of 103

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55.4KZ01.S18G S19G

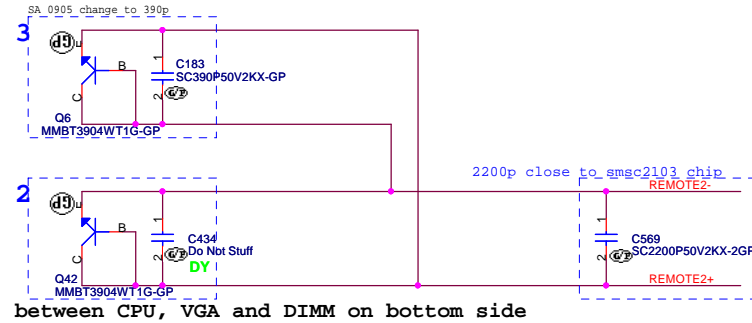
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>LA470</div>	Rev <div>-1</div>
Date: Thursday, November 04, 2010		Sheet 26 of 103



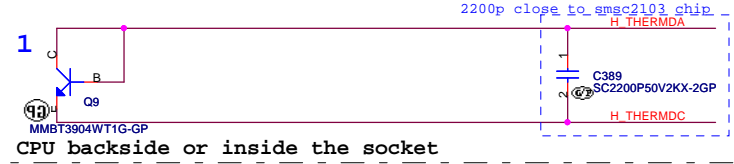
SSID = Thermal

Thermal sensor

Close to PCH on top side.

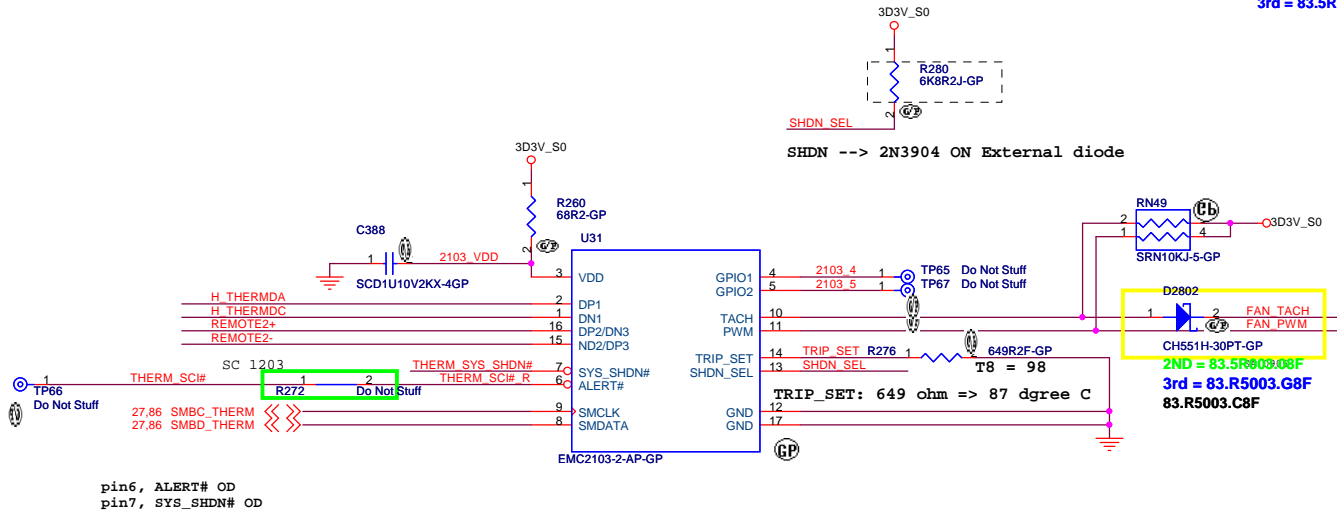
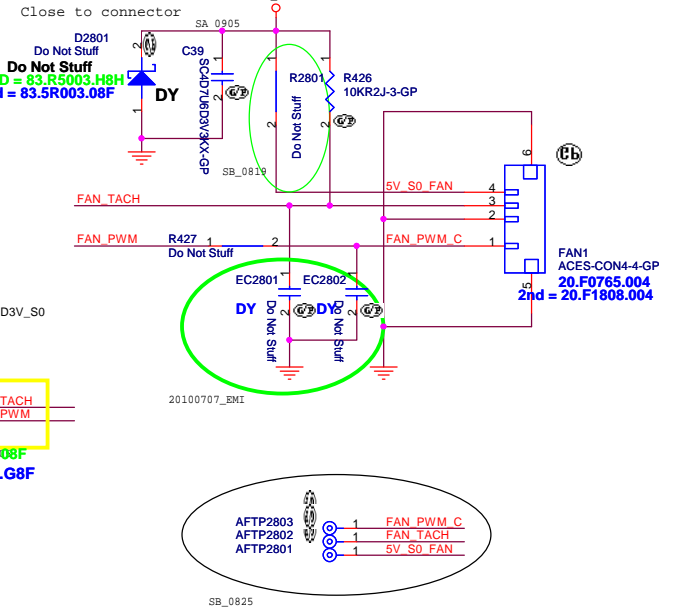


T8

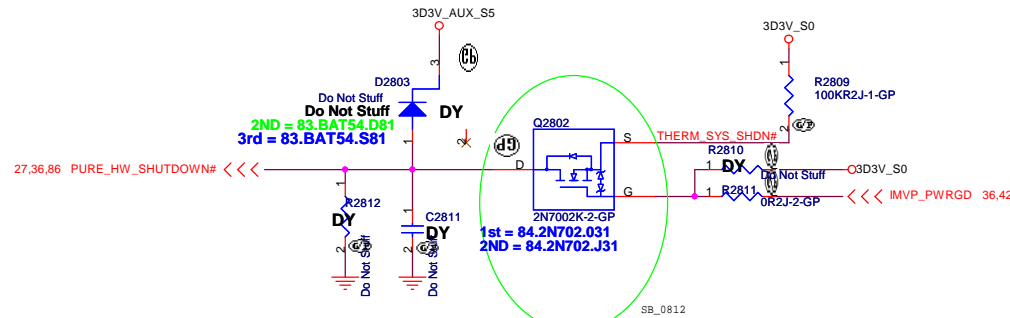


CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width
and spacing. Locate Capacity near Thermal diode.

4 WIRE PWM Fan Control circuit



pin6, ALERT# OD
pin7, SYS_SHDN# OD



55.4KZ01.S18G S19G

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

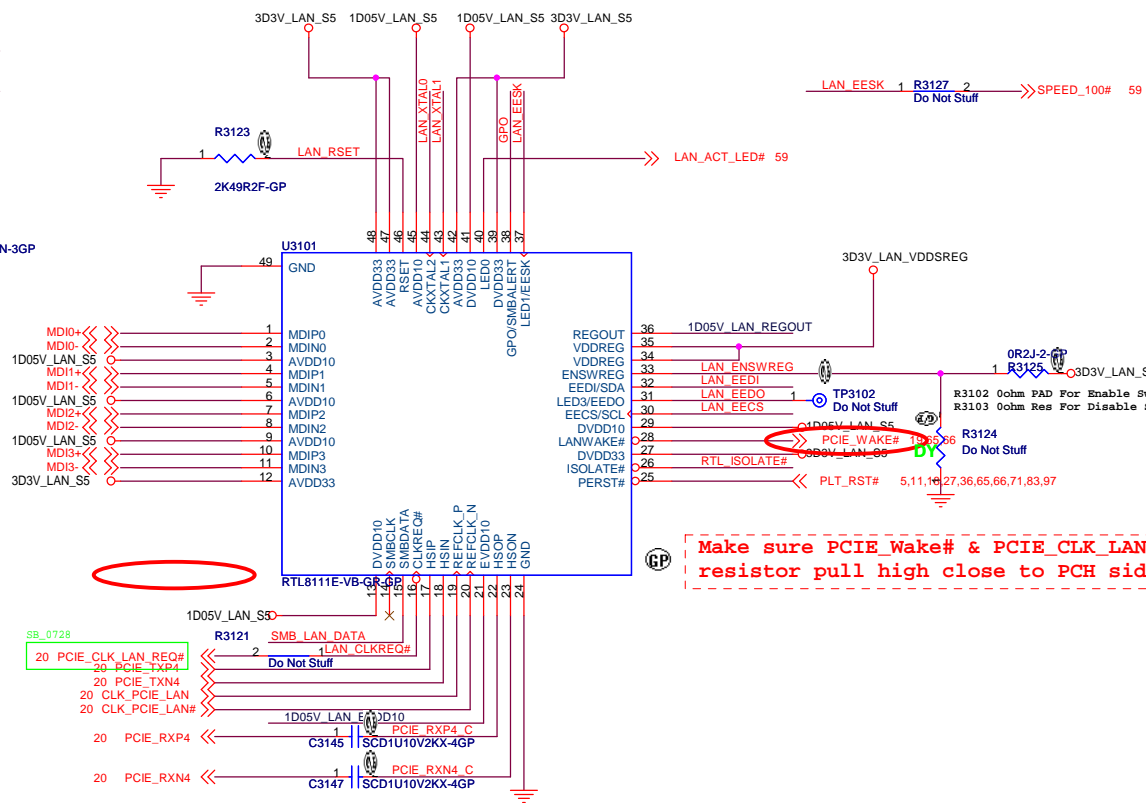
Title			
THERMAL SENSOR SMSC EMC2103			
Size	Document Number	Rev	
A3	LA470	-1	
Date:	Thursday, November 04, 2010	Sheet	28 of 103

55.4KZ01.S18G S19G

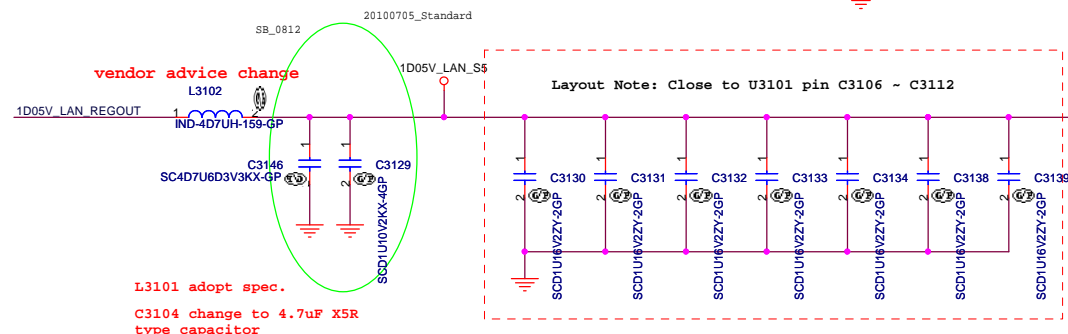
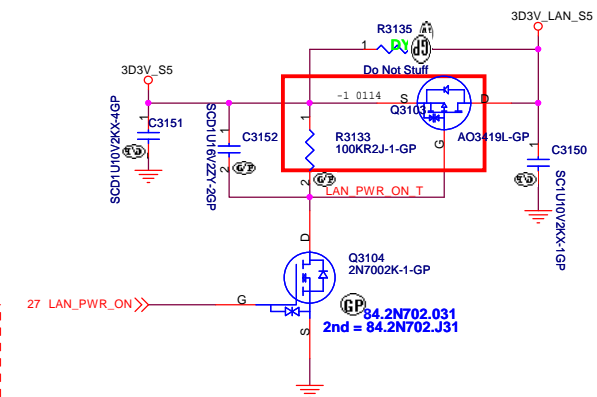
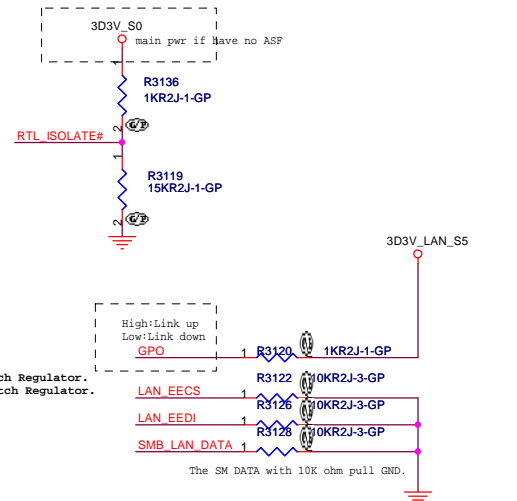
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Audio AMP</div>		
Size <div>A4</div>	Document Number <div>LA470</div>	Rev <div>-1</div>
Date: Thursday, November 04, 2010		Sheet 30 of 103

[illegible]

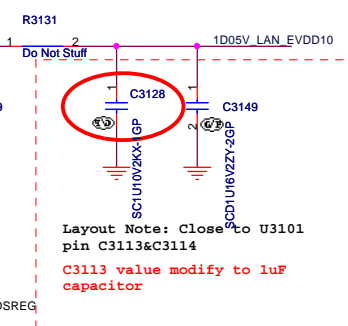
Pin-XTAL2 is External Clock Input Pin.
R3121 is need when using external clock source.



Make sure PCIE_Wake# & PCIE_CLK_LAN resistor pull high close to PCH side

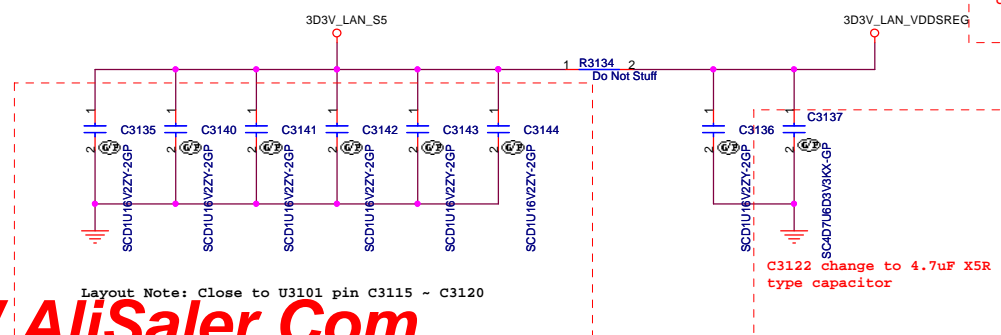


L3101 adopt spec.
C3104 change to 4.7uF X5R
type capacitor



Layout Note: Close to U3101
pin C3113&C3114

C3113 value modify to 1uF
capacitor



Layout Note: Close to U3101 pin C3115 ~ C3120

55.4KZ01.S18G S19G

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Title			
LAN RTL8111E			
Size A3	Document Number		Rev
	LA470		-1
Date:	Thursday, November 04, 2010	Sheet 31 of	103



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55.4KZ01.S18G S19G		
<div>緯創資通Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
RTS5159 (CARD READER)		
Size	Document Number	Rev
A3	LA470	-1
Date:	Thursday, November 04, 2010	Sheet 32 of 103

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55.4KZ01.S18G S19G

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>LA470</div>	Rev <div>-1</div>
Date: Thursday, November 04, 2010		Sheet 33 of 103

(Blanking)

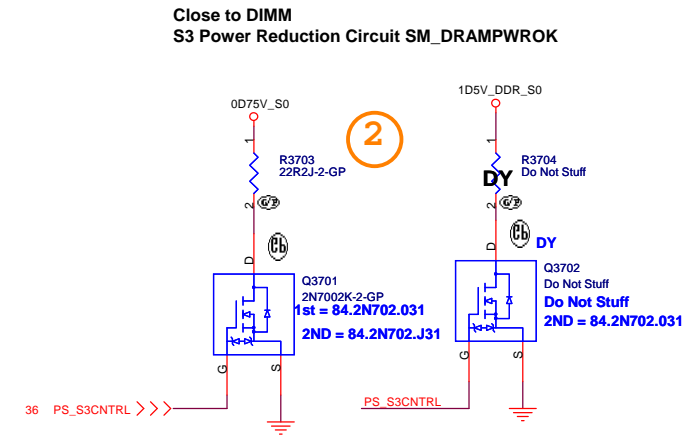
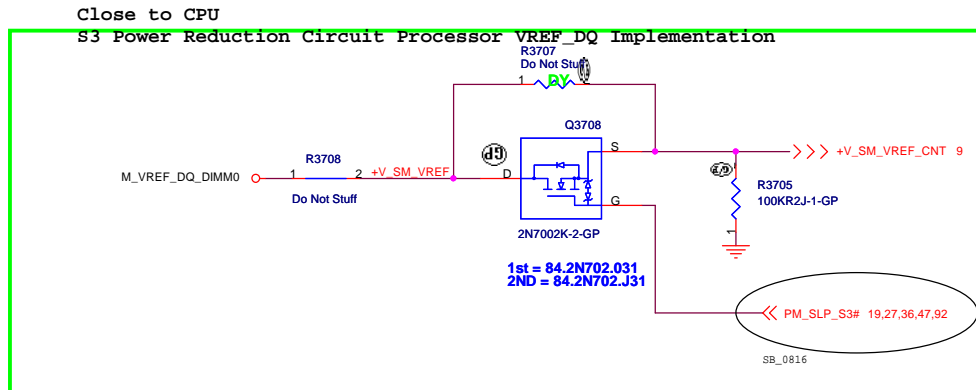
55.4KZ01.S18G S19G

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>LA470</div>	Rev <div>-1</div>
Date: Thursday, November 04, 2010		Sheet 34 of 103

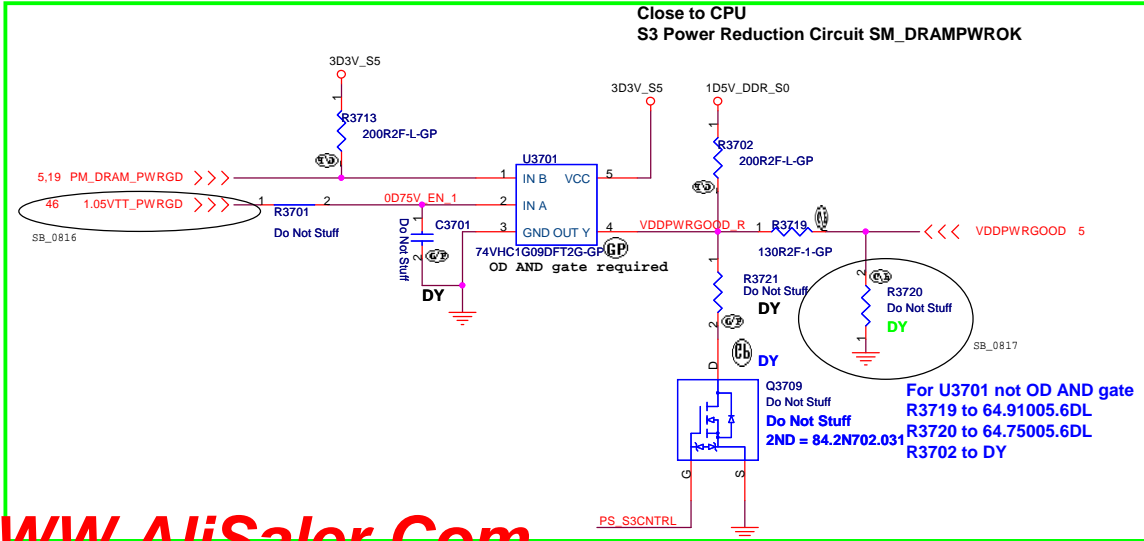
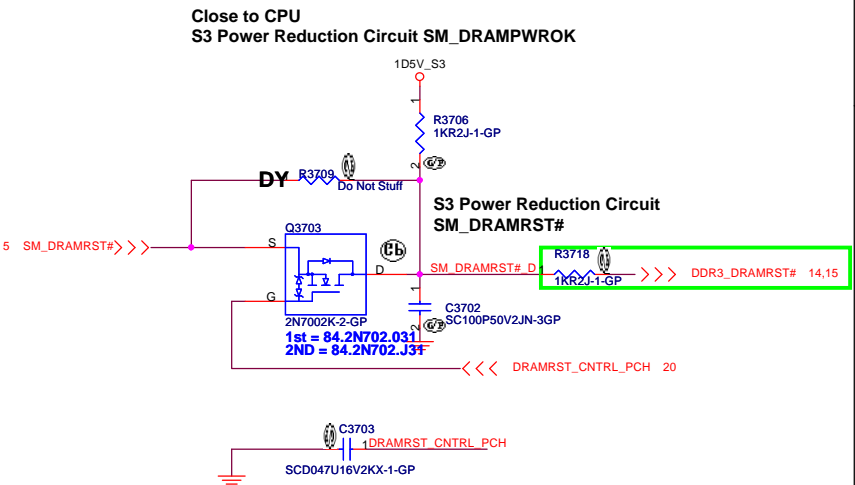
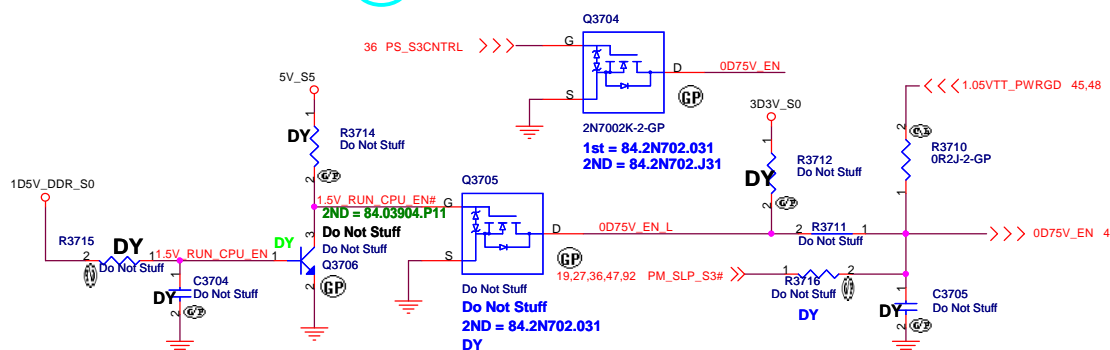
5	4	3	2	1
D				
C				
B				
A				

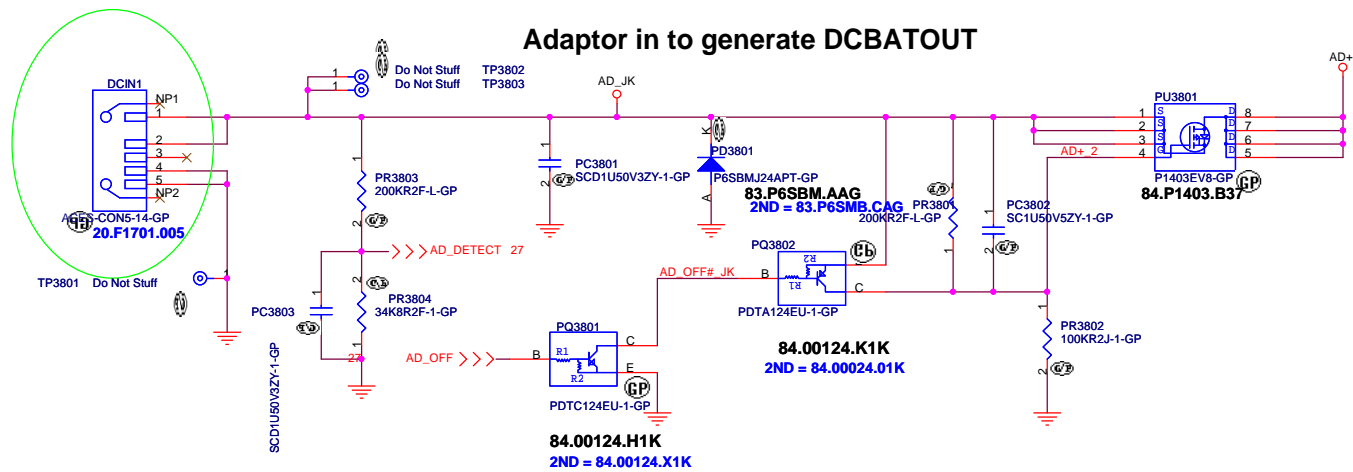
55.4KZ01.S18G S19G

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB 3.0 Controller			
Size	Document Number		Rev
A3	LA470		-1
Date:	Thursday, November 04, 2010	Sheet	35 of 103



5 S3 Power Reduction X01 20091111

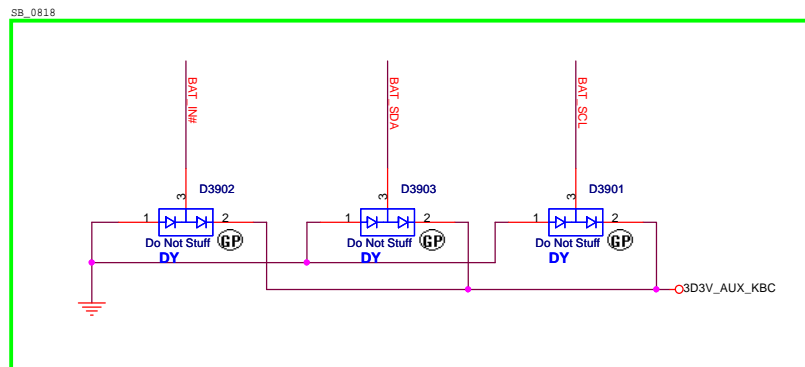
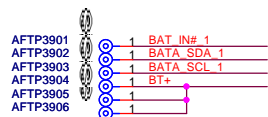
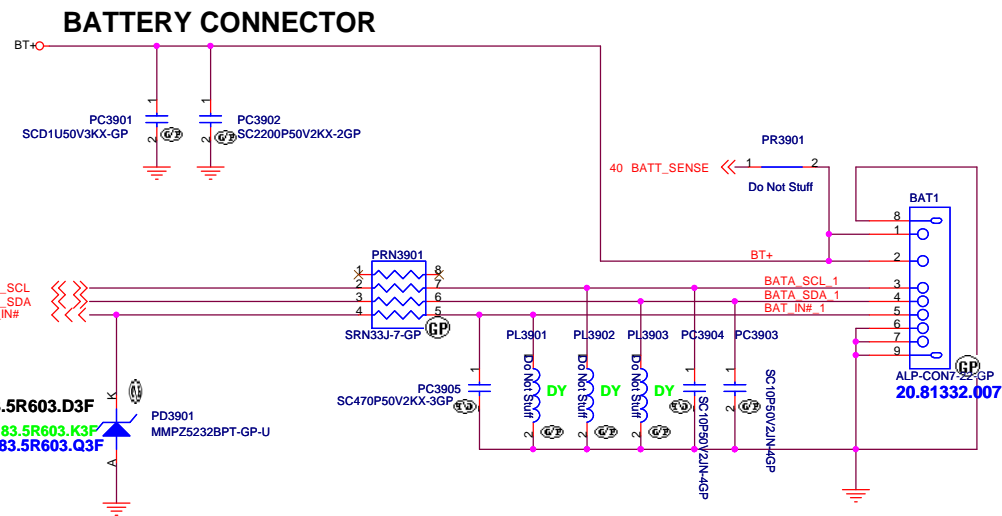




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緯創資通 Wistron Corporation
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Title		DCIN_JACK	
Size	Document Number	LA470	
Date:	Thursday, November 04, 2010	Sheet	38 of 103
Rev		-1	

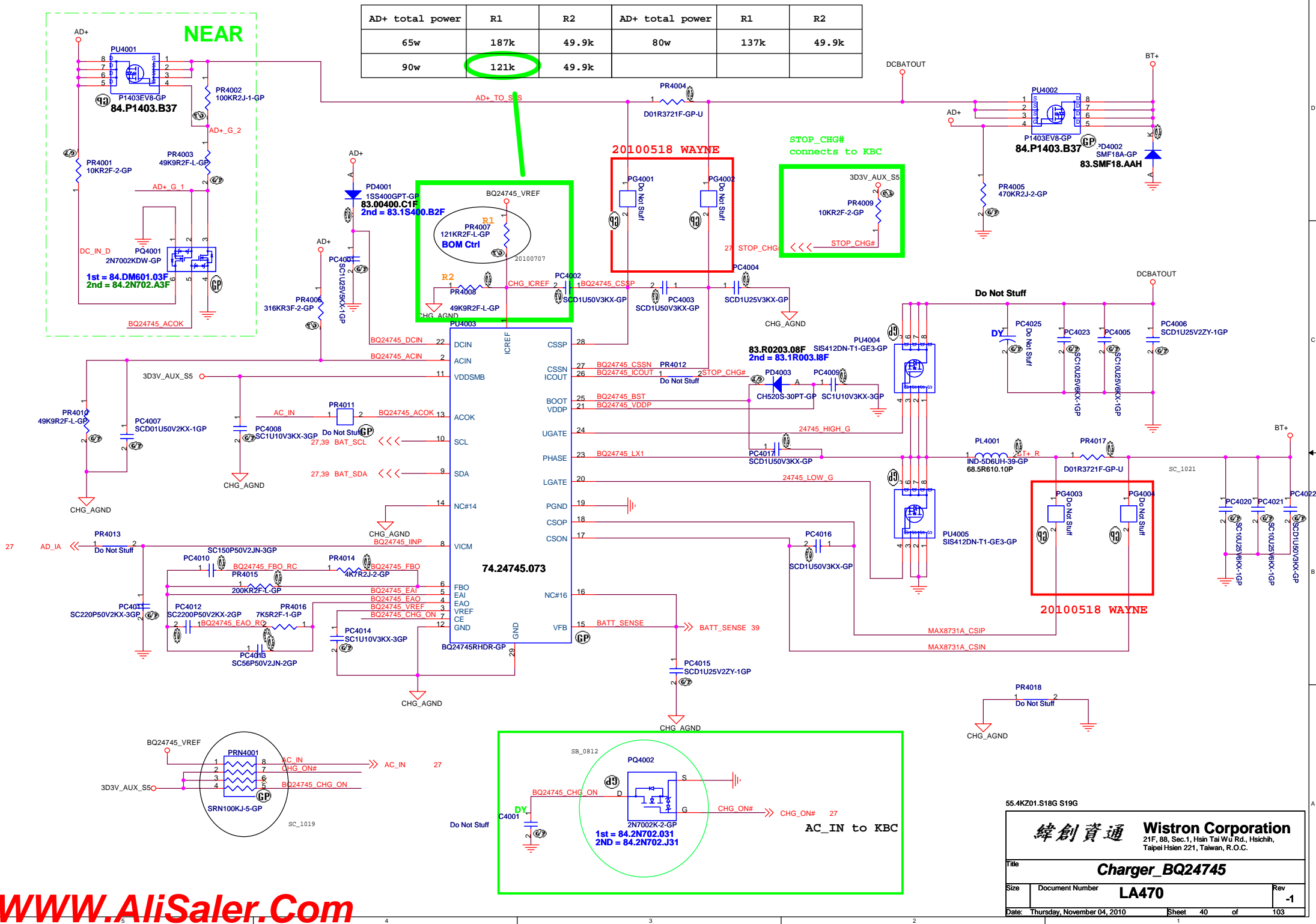


DY ???

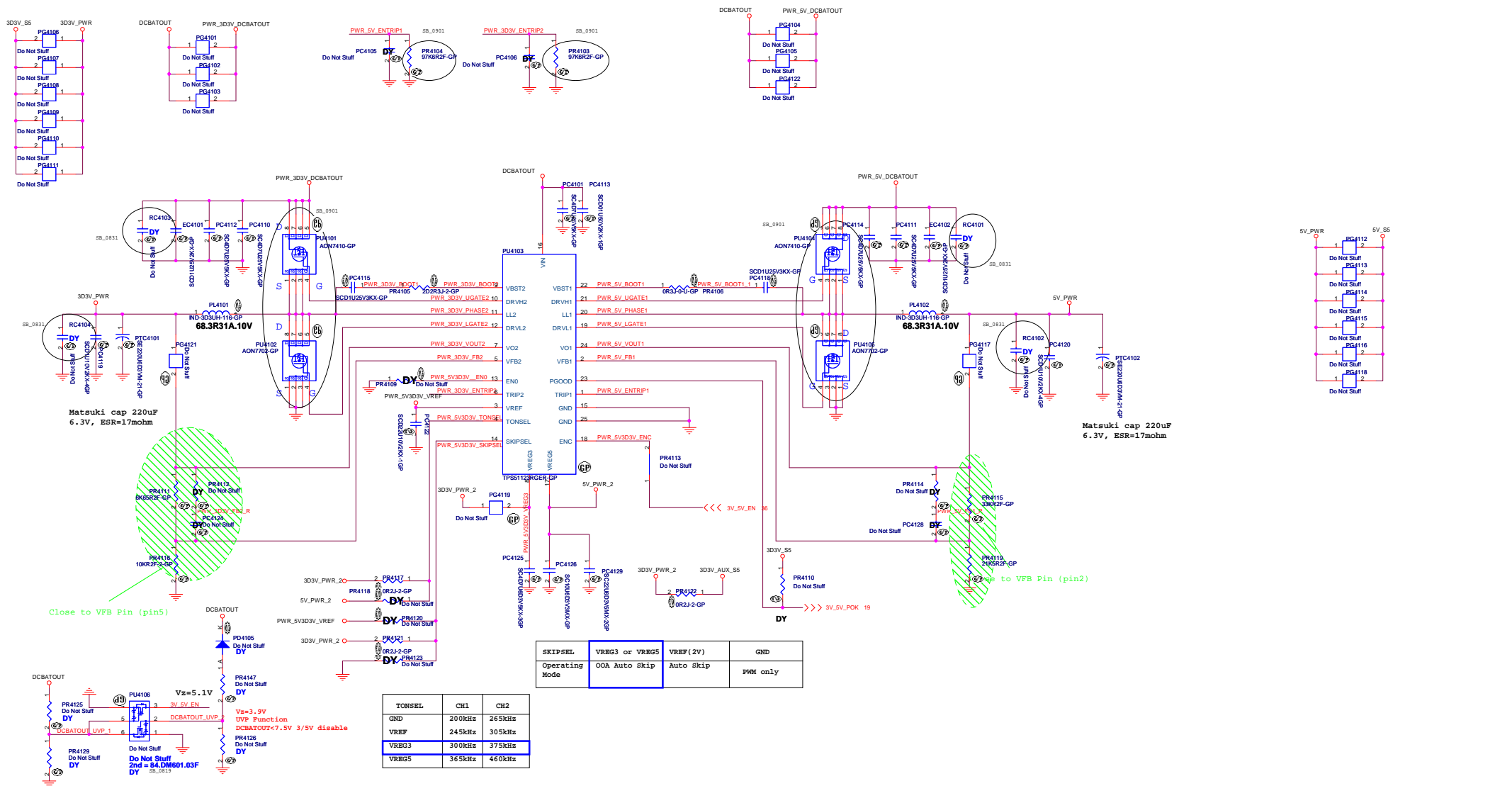
55.4KZ01.S18G S19G

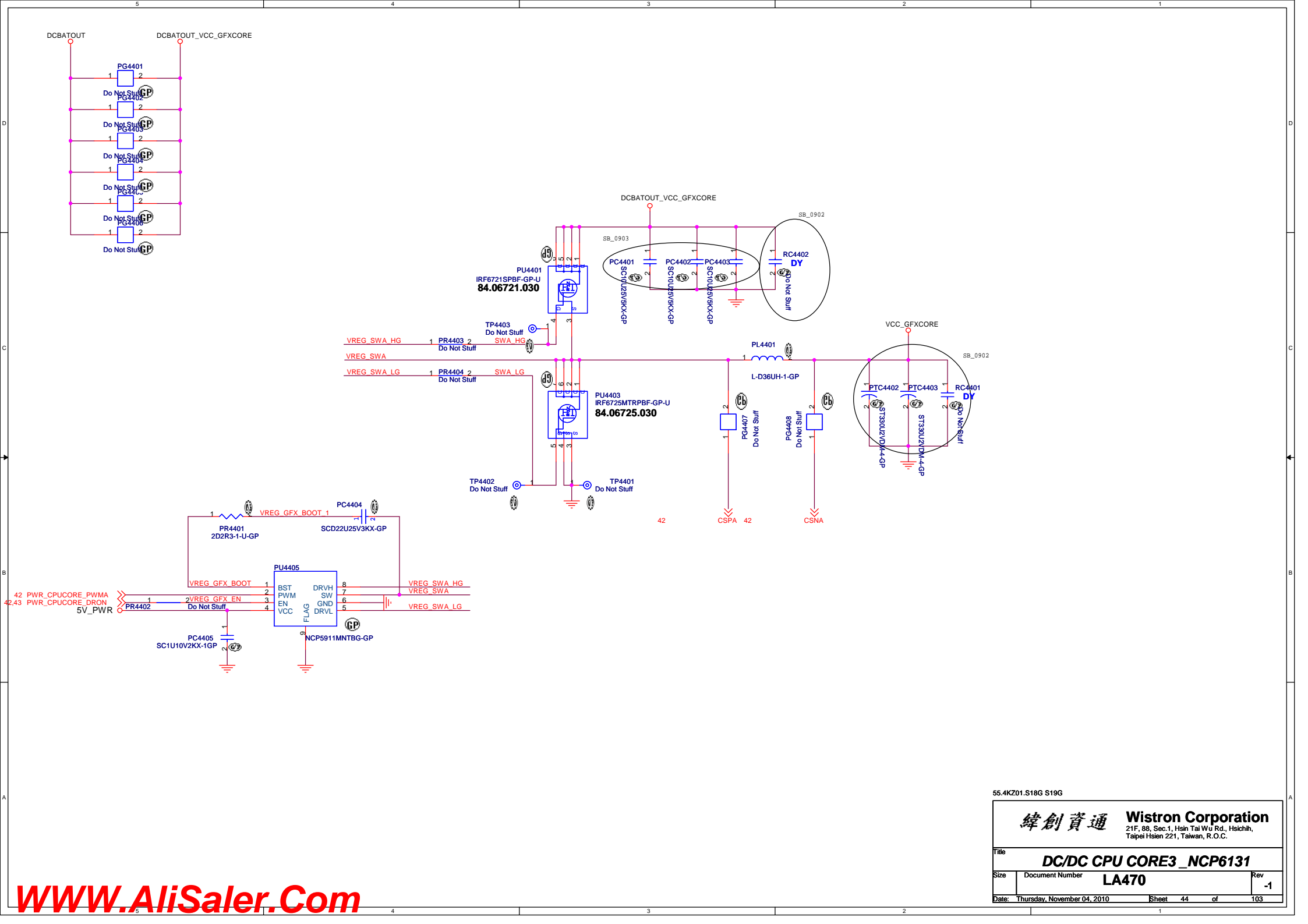
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	BATT_CONN
Size	Document Number LA470
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Rev	-1

AD+ total power	R1	R2	AD+ total power	R1	R2
65w	187k	49.9k	80w	137k	49.9k
90w	121k	49.9k			



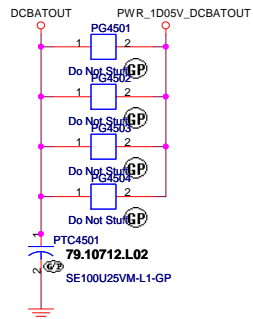
SSID = PWR.Plane.Regulator_5v3p3v



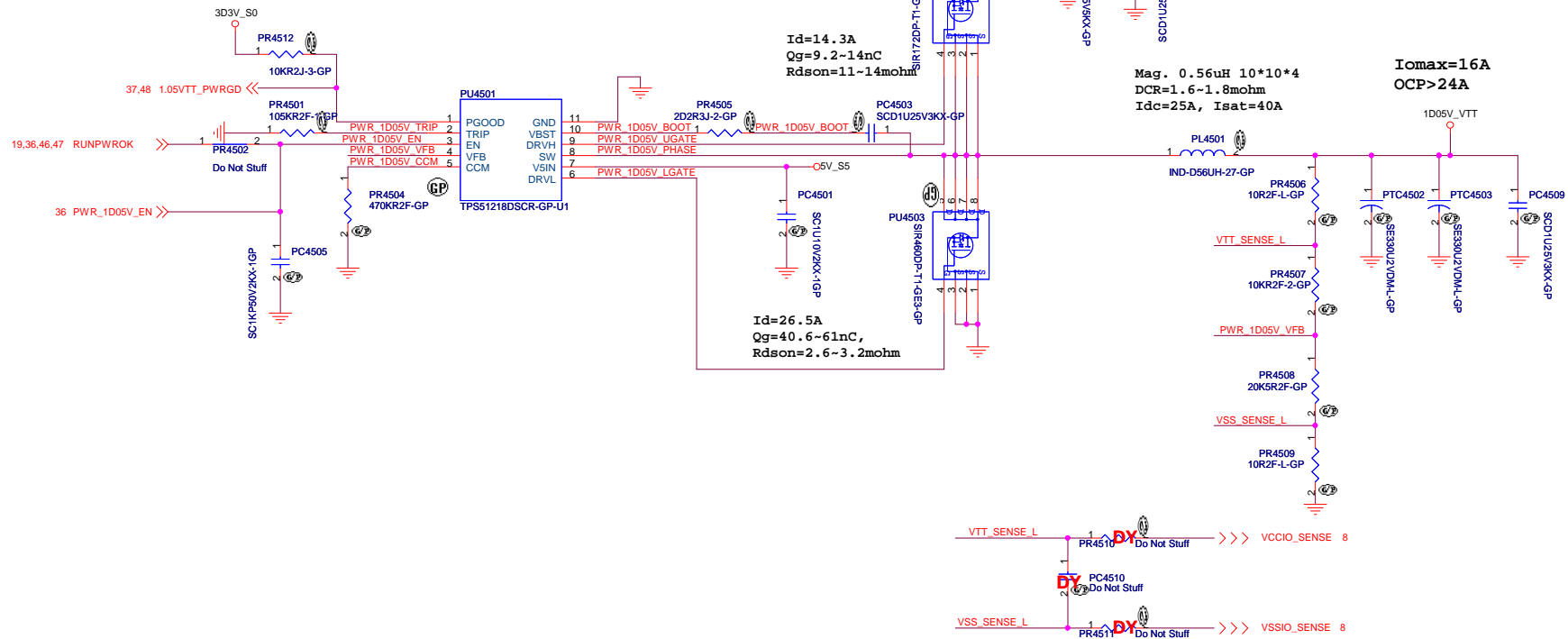


55.4KZ01.S18G S19G

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
DC/DC CPU CORE3_NCP6131			
Size	Document Number		Rev
	LA470		-1
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TPS51218 for 1D05V

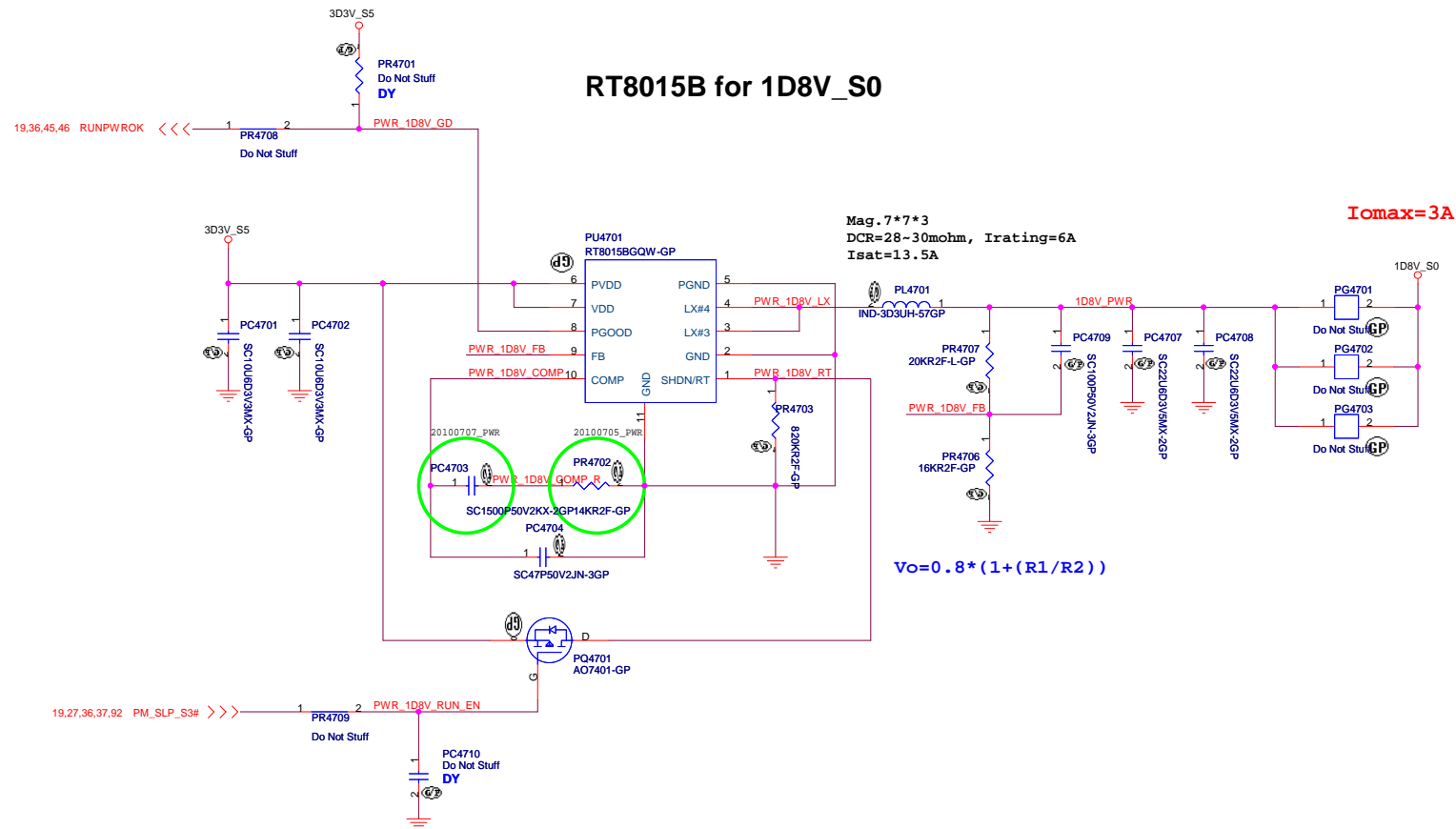


$$V_{out} = 0.704V * (R1 + R2) / R2$$

55.4KZ01.S18G S19G

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

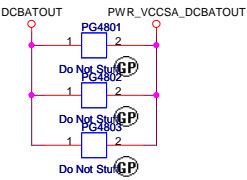
Title		
TPS51218_1D05V		
Size	Document Number	Rev
		-1
Date:	Thursday, November 04, 2010	Sheet 45 of 103



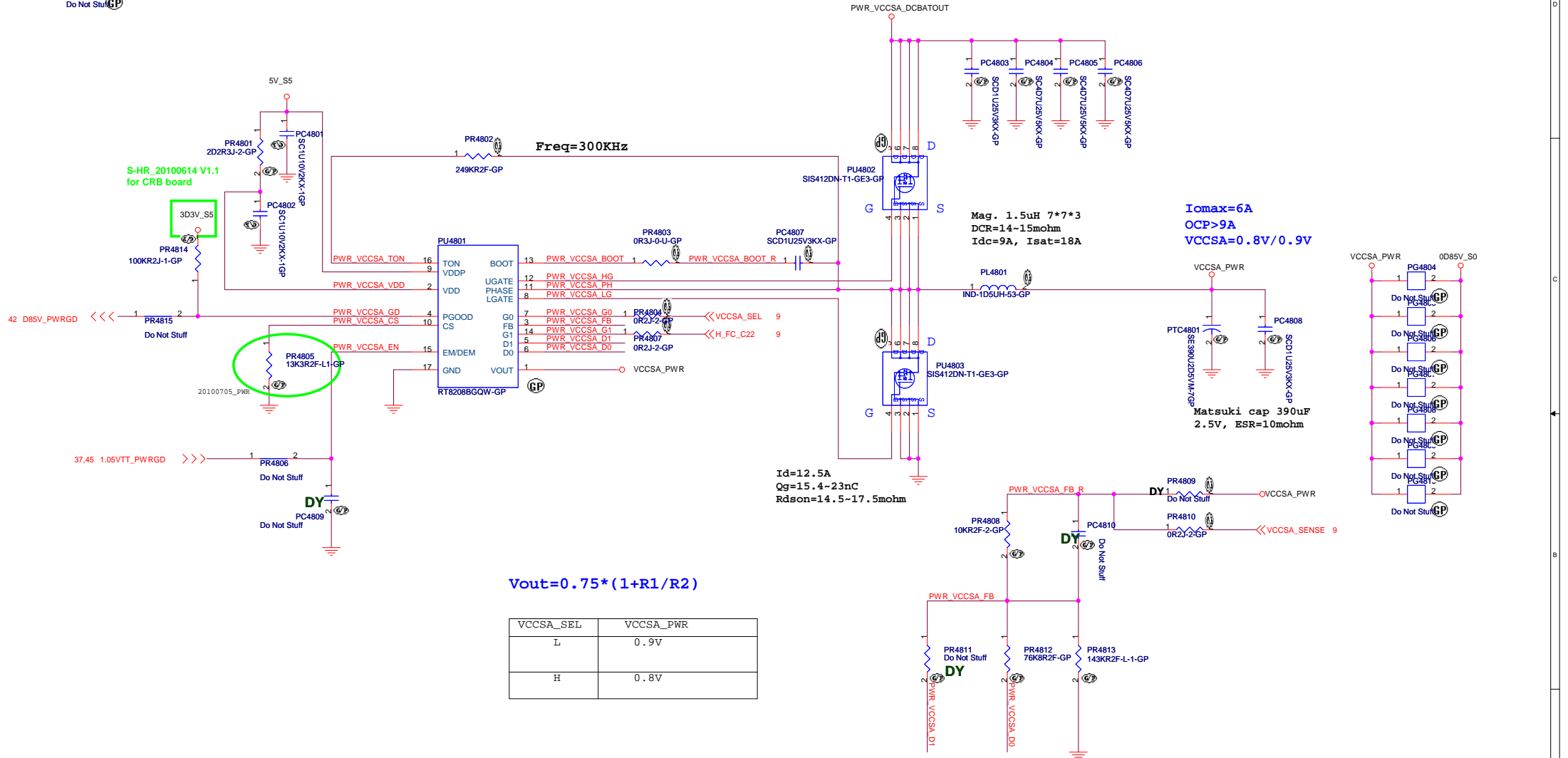
55.4KZ01.S18G S19G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		PWM_1D8V_RT8015B	
Size	Document Number	LA470	
Date	Thursday, November 04, 2010	Sheet	47 of 103
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RT8208A for VCCSA



55.4KZ01.S18G S19G

緯創資通

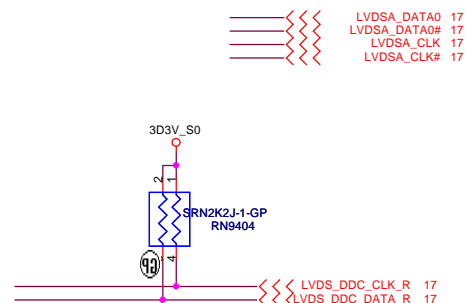
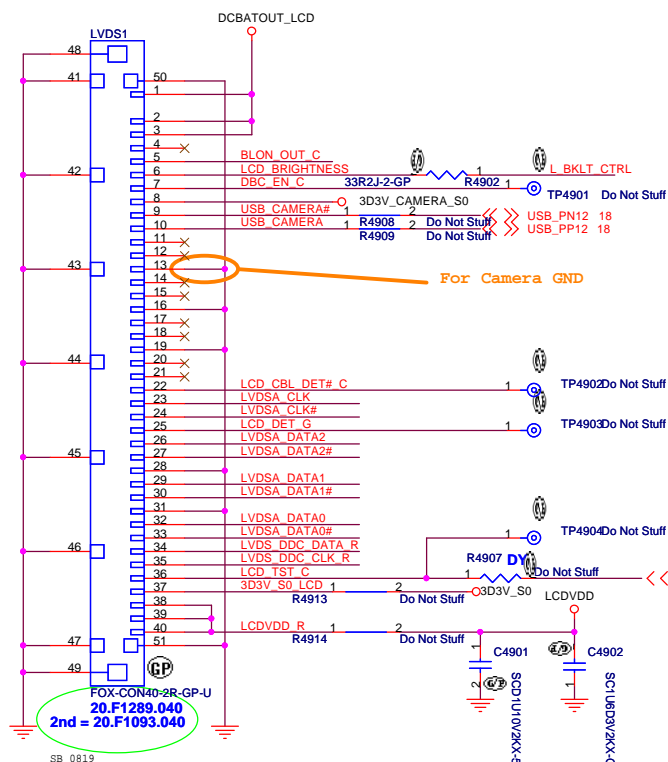
Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

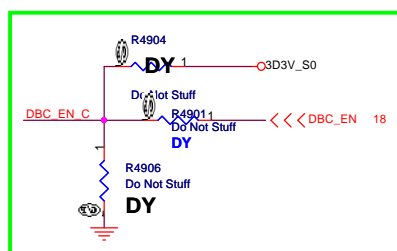
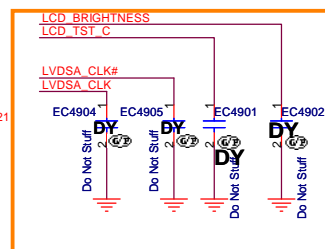
Title RT8208B_VCCSA		
Size	Document Number LA470	Rev -1
Date: Thursday, November 04, 2010	Sheet 48 of	103

SSID = VIDEO

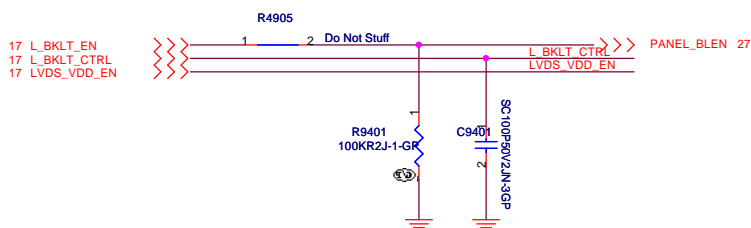
LVDS CONNECTOR



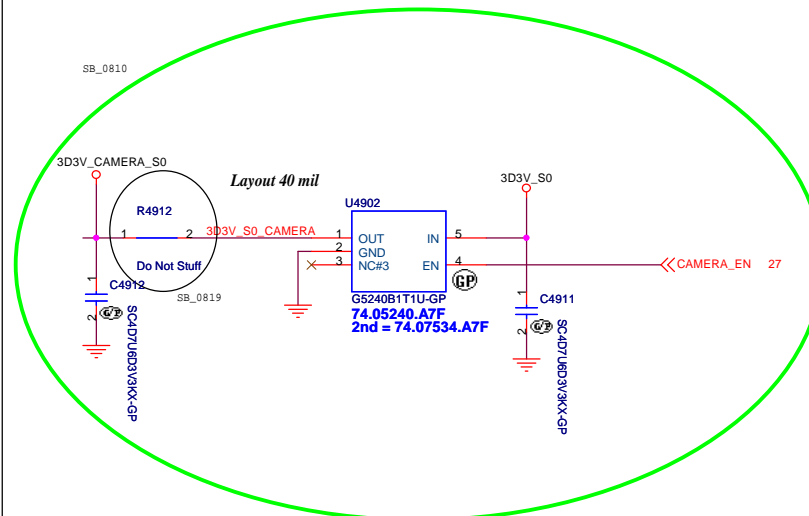
For EMI request
Close to LVDS connector



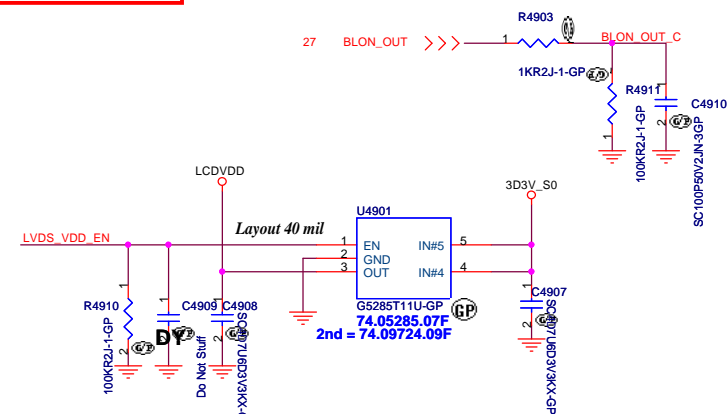
Panel BL brightness/Power En/BL En



CAMERA POWER



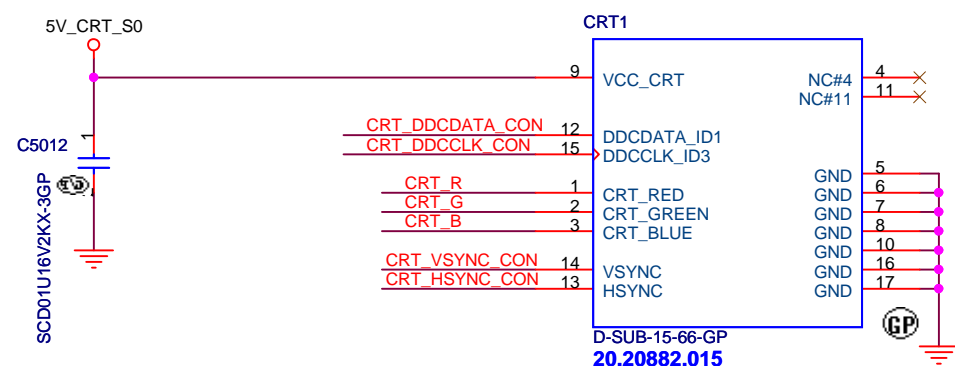
SSID = VIDEO



55.4KZ01.S18G S19G

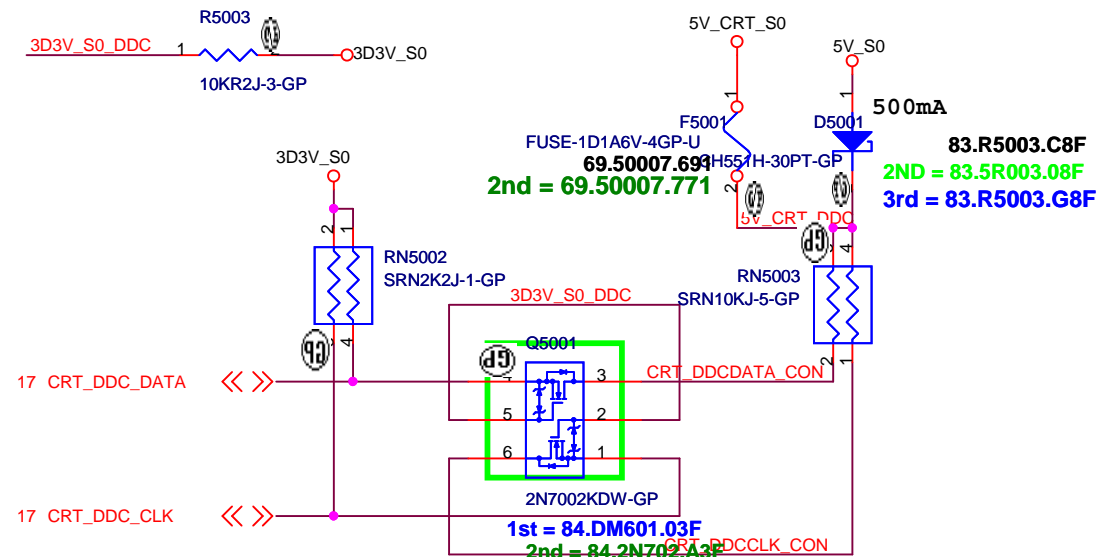
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
LCD Connector			
Size A3	Document Number LA470		Rev -1
Date	Thursday, November 04, 2010		Sheet 49 of 103

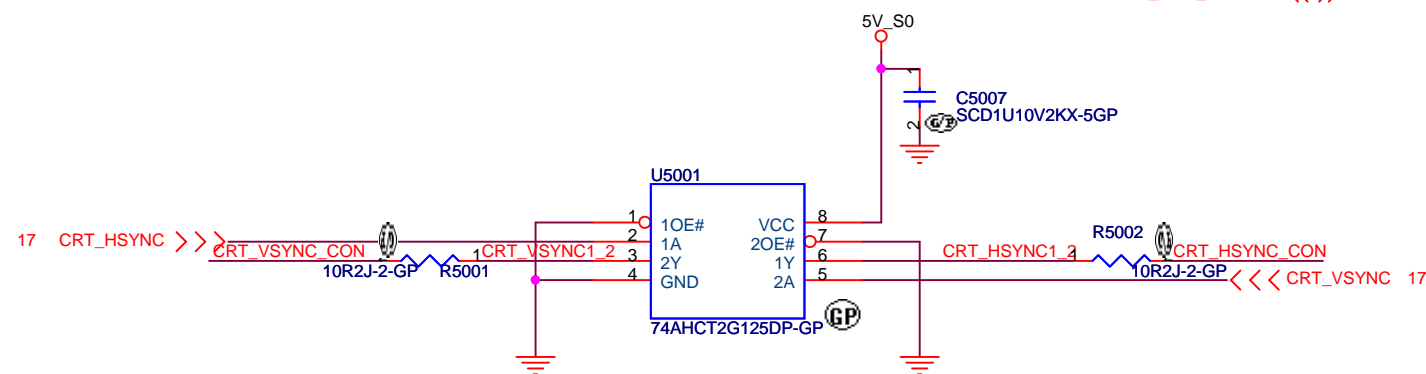


CRT DDCDATA & DDCCLK level shift

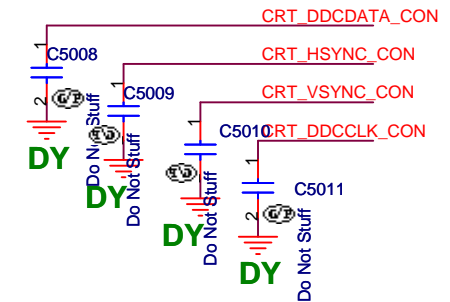
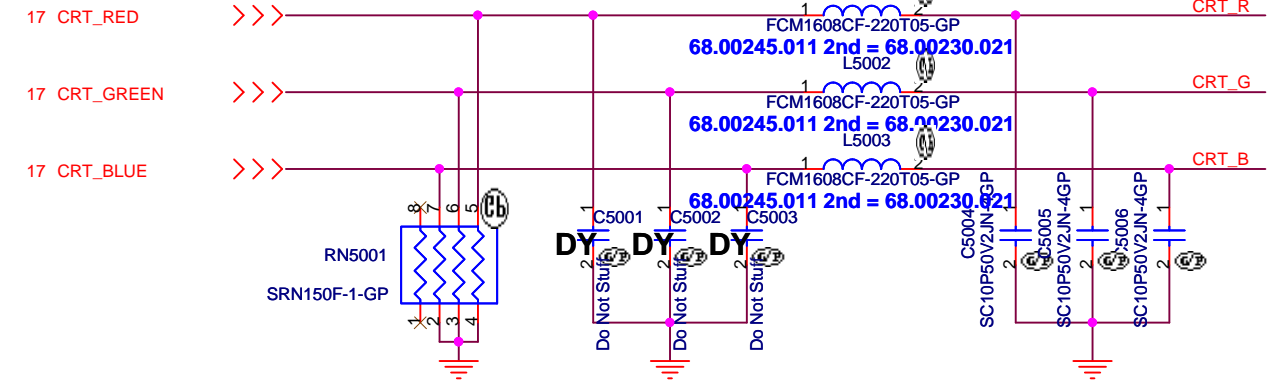
Pull High 5V Design on CRT Board



CRT Hsync & Vsync level shift



CRT RGB



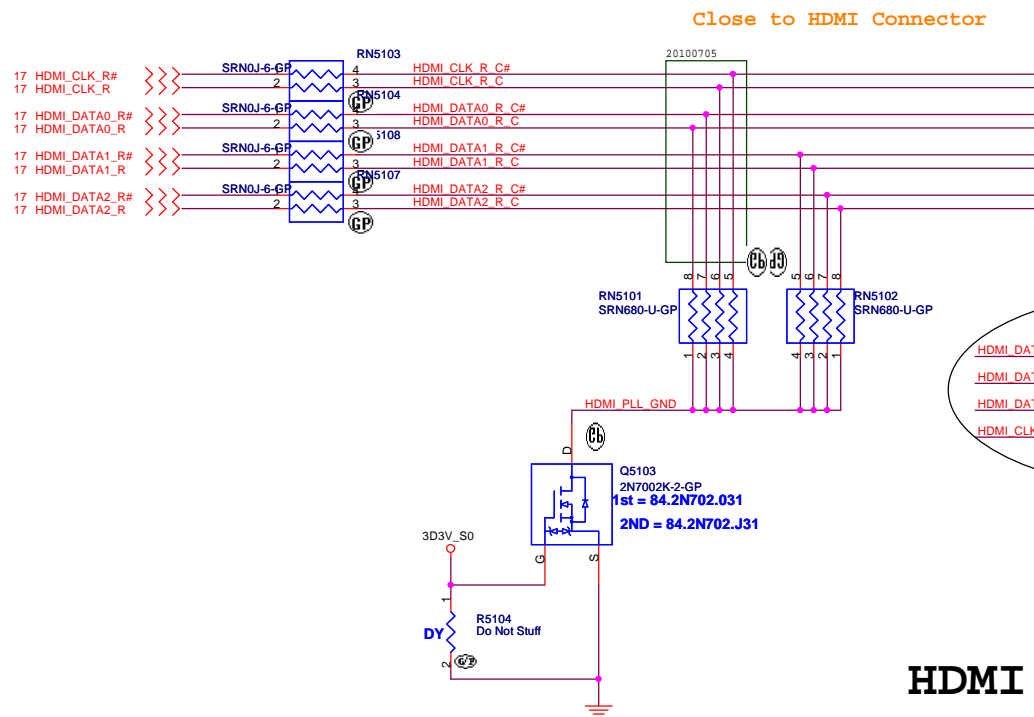
55.4KZ01.S18G S19G

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CRT Connector	
Size A4	Document Number LA470
Date Thursday, November 04, 2010	Sheet 50 of 103
Rev -1	

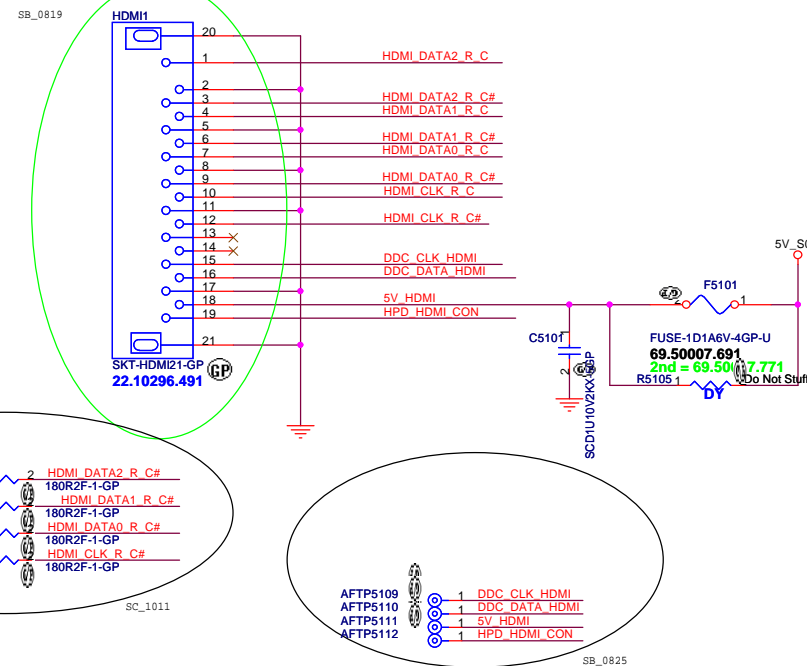
SSID = VIDEO

HDMI CONNECTOR

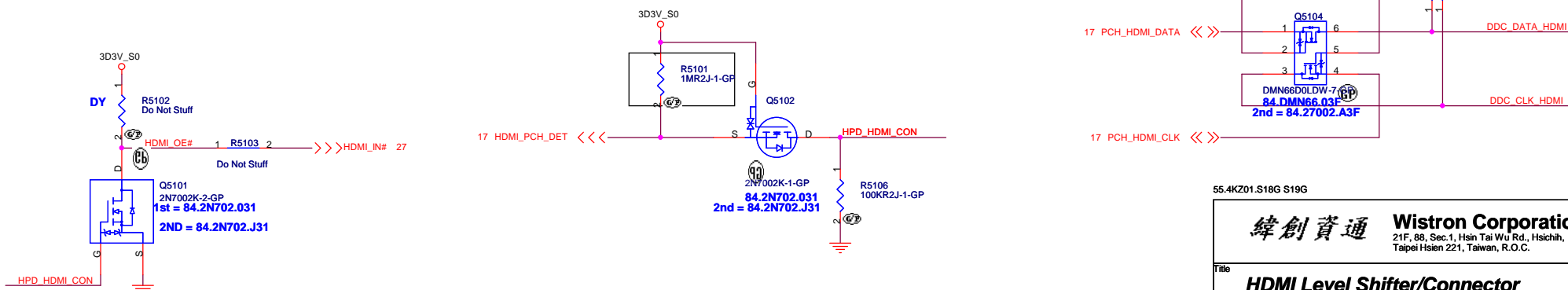
HDMI Passive Level Shifter



HDMI CONN



HDMI DDC Passive Level Shifter



緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
HDMI Level Shifter/Connector		
Size	Document Number	Rev
A3	LA470	-1
Date:	Thursday, November 04, 2010	Sheet 51 of 103

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55.4KZ01.S18G S19G

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
eDP			
Size	Document Number		Rev
A3	LA470		-1
Date:	Thursday, November 04, 2010		Sheet 52 of 103

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55.4KZ01.S18G S19G

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>S-VIDEO</div>		
Size <div>A4</div>	Document Number <div>LA470</div>	Rev <div>-1</div>
Date: Thursday, November 04, 2010		Sheet 53 of 103

(Blanking)

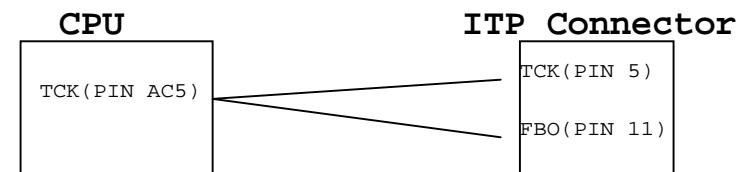
55.4KZ01.S18G S19G

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>LA470</div>	Rev <div>-1</div>
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SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



55.4KZ01.S18G S19G

緯創資通

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Title

ITP

Size
A4

Document Number

LA470

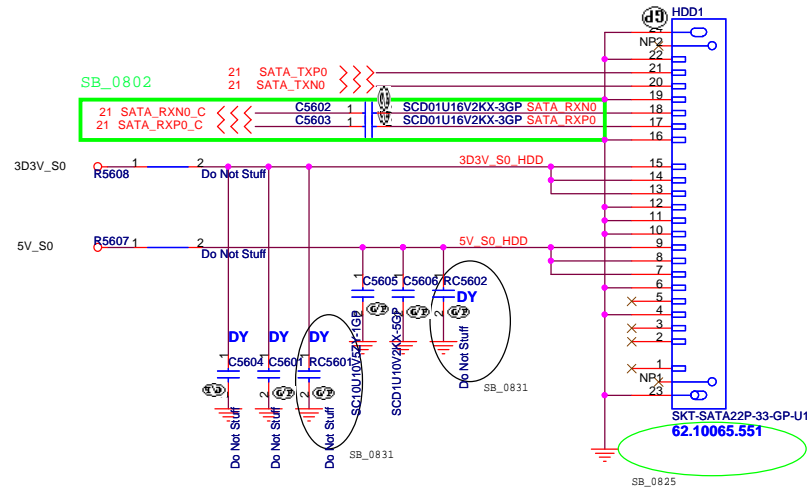
Rev
-1

Date: Thursday, November 04, 2010

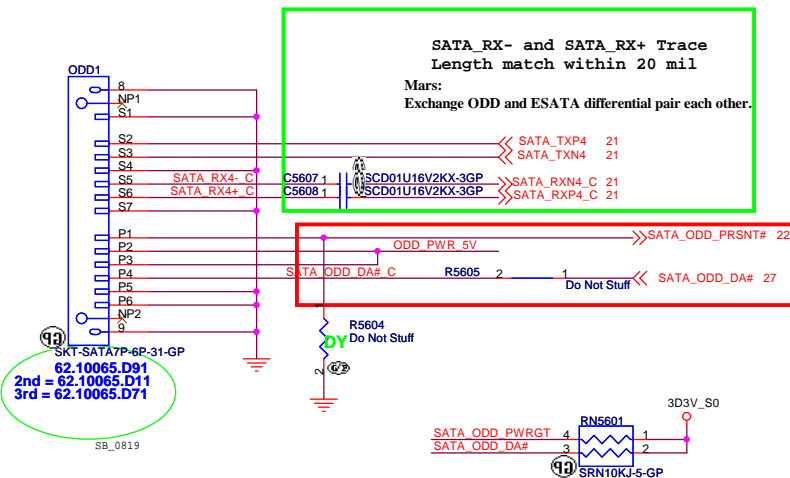
Sheet 55 of 103

SSID = SATA

SATA HDD Connector

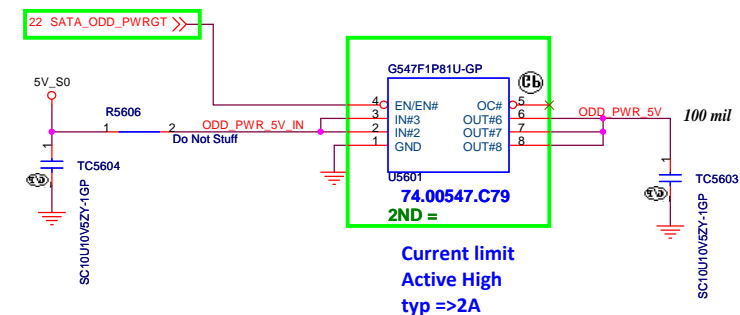


ODD Connector



SUPPORT ZERO SATA ODD

SATA Zero Power ODD



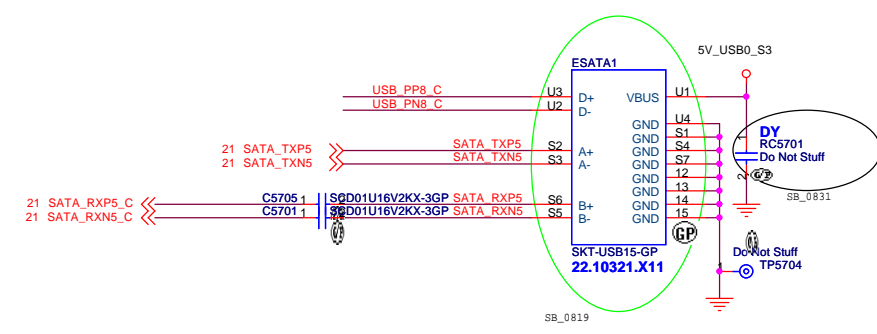
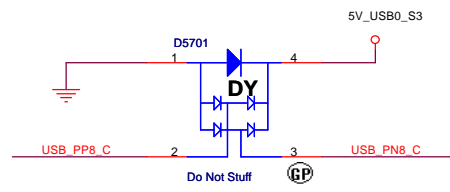
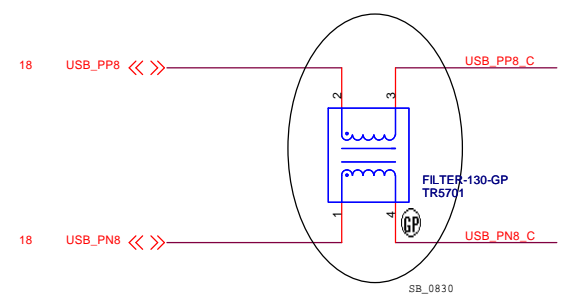
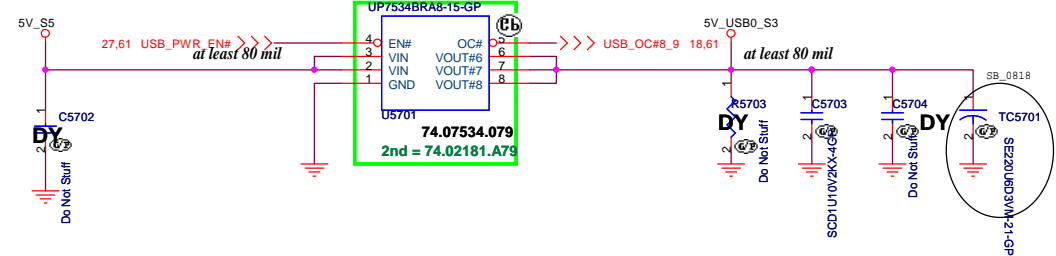
55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
HDD/ODD			
Size A3	Document Number		Rev
	LA470		-1
Date:	Thursday, November 04, 2010		Sheet 56 of 103

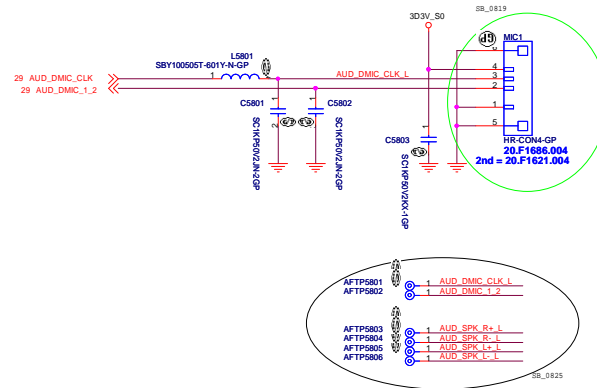
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USB Power



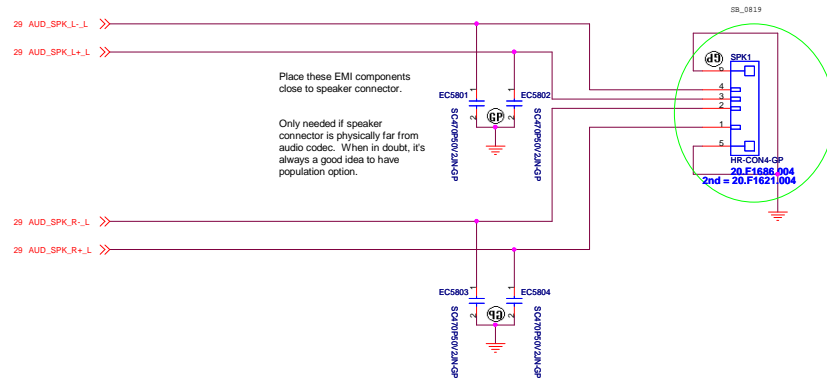
Do Not Stuff

TP5701	1	5V_USB0_S3
TP5702	1	USB_PN8_C
TP5703	1	USB_PP8_C



INTERNAL STEREO SPEAKERS

Port G



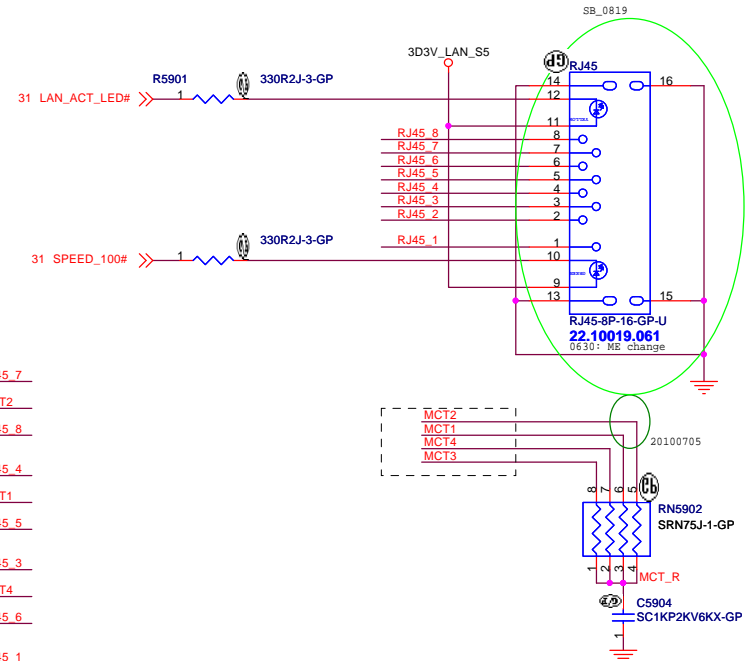
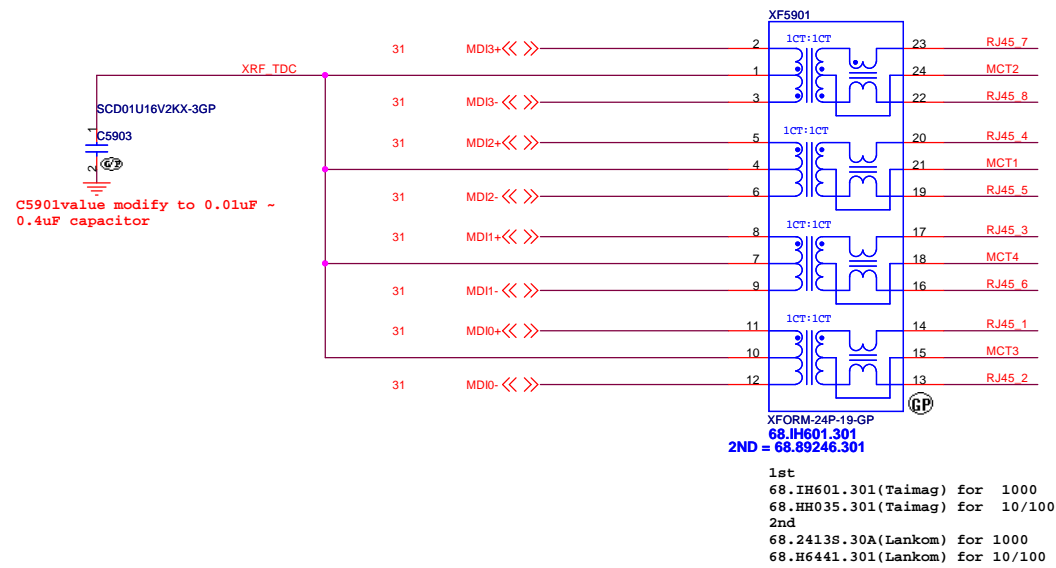
55-4KZ01.S18G S18G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title			MIC/SPEAKER/AUDIO JACK
Size	Document Number	Rev	-1
K2	LA470		
Date:	Thursday, November 04, 2010	Sheet	58 of 109

LAN Connector

FOR CO-LAY GIGA Lan Transformer



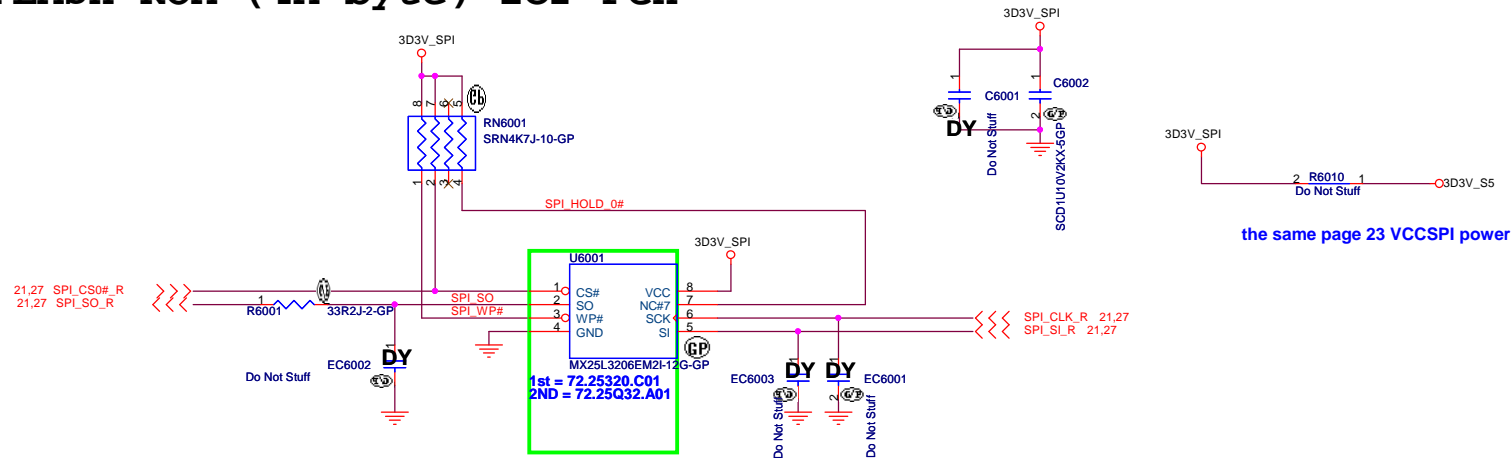
55.4KZ01.S18G S19G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

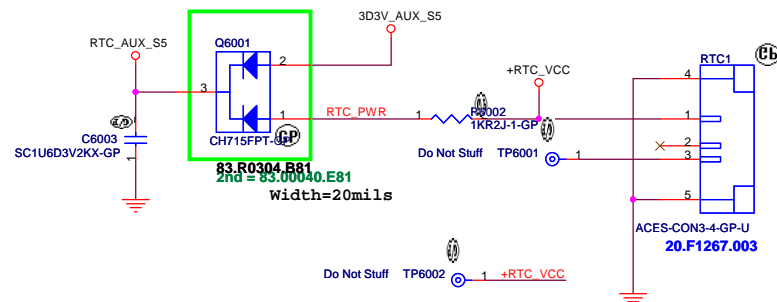
Title		
RJ45 / Transformer		
Size	Document Number	Rev
A3	LA470	-1
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```
SSID = Flash.ROM
```

SPI FLASH ROM (4M byte) for PCH



SSID = RBATT



55.4KZ01.S18G S19G

緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Flash/RTCSize
A3

	Document Number
--	-----------------

Rev
-1

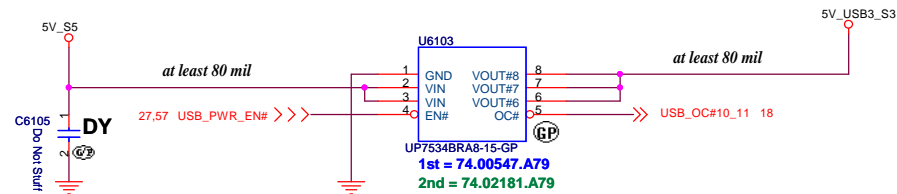
Rev

-1

11

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Sub-USB Board Power



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Taipei Hsien 221, Taiwan, R.O.C.

USB Power SW

LA470

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55.4KZ01.S18G S19G

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB 3.0 Port			
Size	Document Number		Rev
A3	LA470		-1
Date:	Thursday, November 04, 2010		Sheet 62 of 103

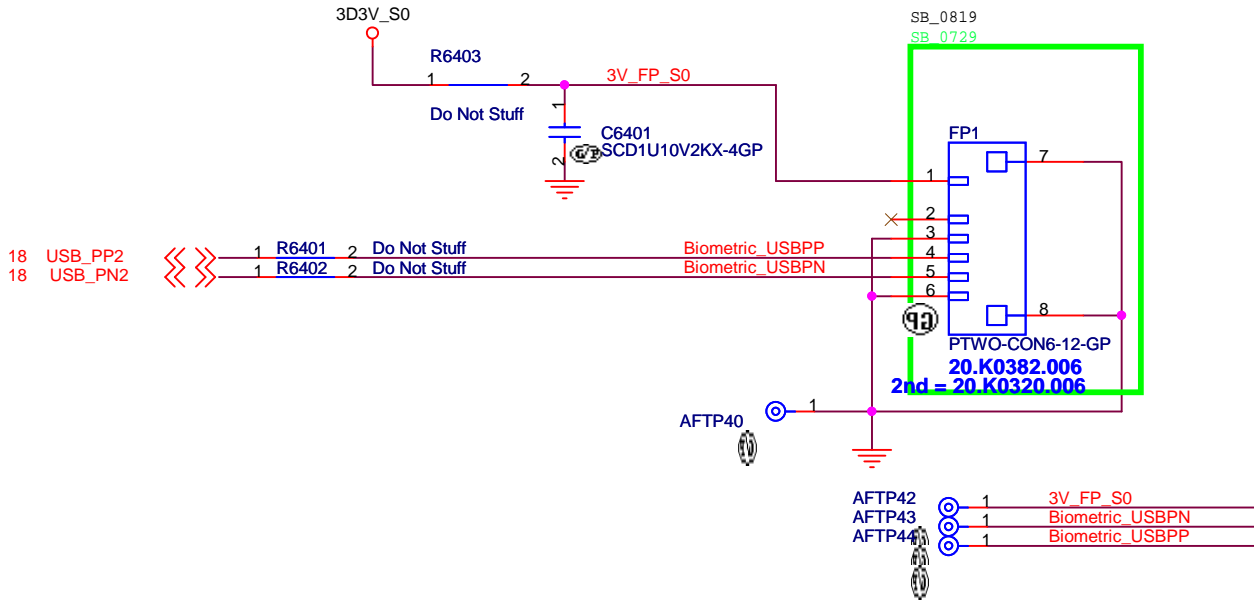
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緯創資通

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Finger Printer Connector



55.4KZ01.S18G S19G

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

RESERVED

Size

Document Number

LA470

Rev

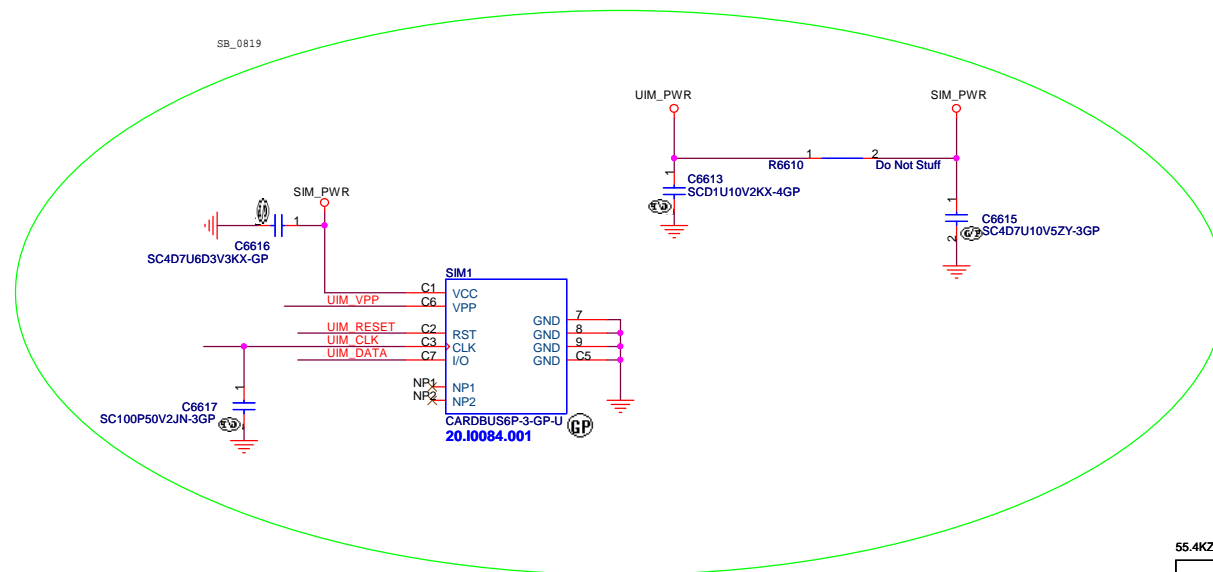
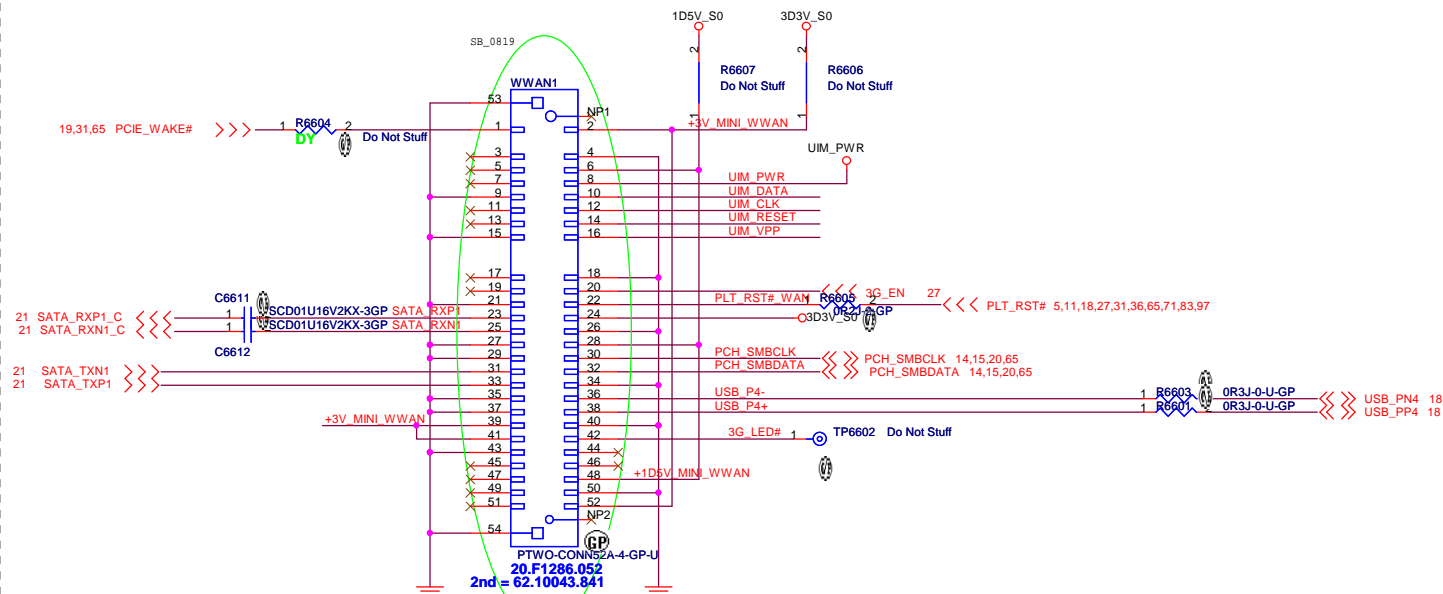
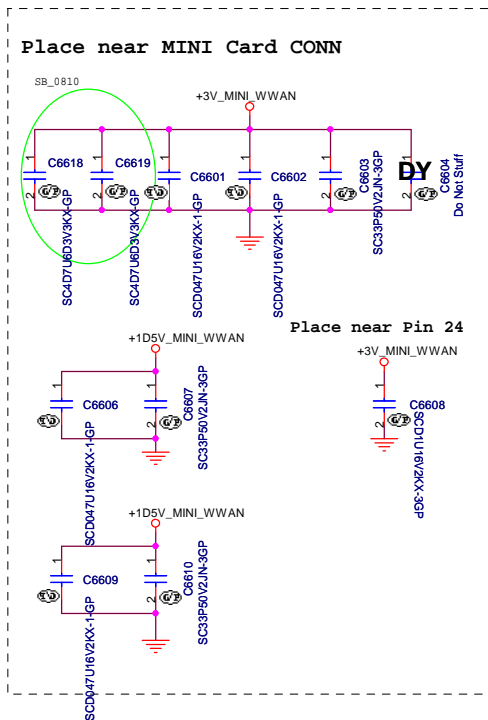
-1

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Mini Card Connector(WWAN)



55.4KZ01.S18G S19G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

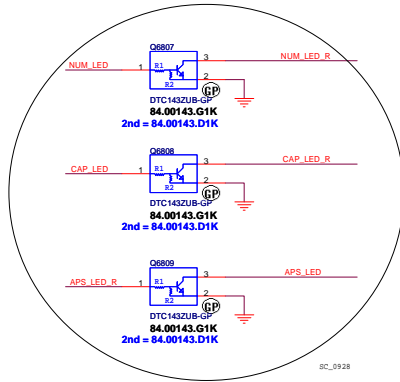
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WWAN Connector			
Size A3	Document Number LA470	Rev -1	
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55.4KZ01.S18G S19G

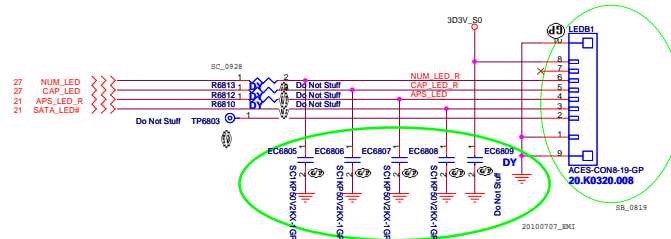
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Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>LA470</div>	Rev <div>-1</div>
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Power button LED

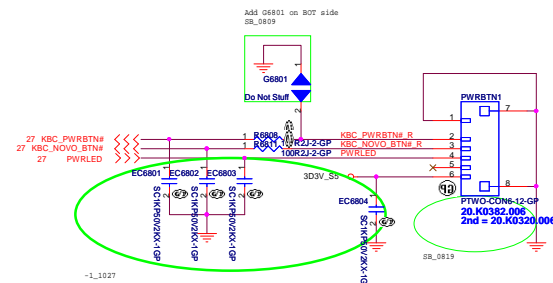


SR_0928

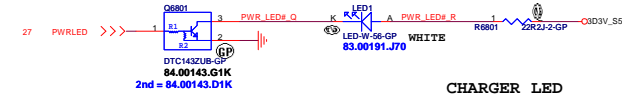
LED Bord CONN.



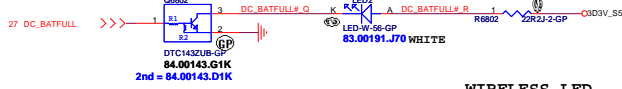
Power button LED(White)



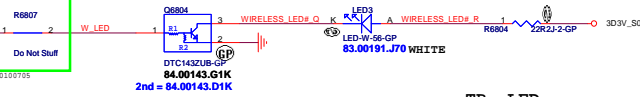
POWER LED



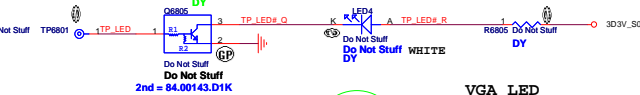
CHARGER LED



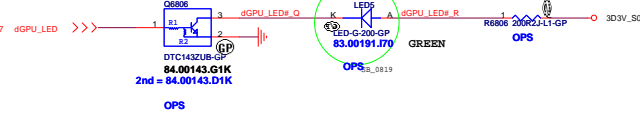
WIRELESS_LED



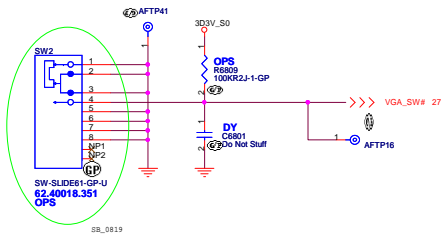
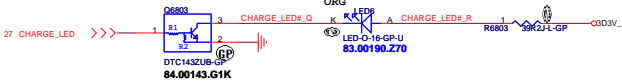
TP_LED



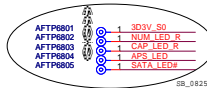
VGA_LED



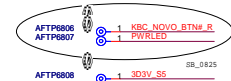
CHARGER LED ORG



SR_0819



SR_0825



SR_0825

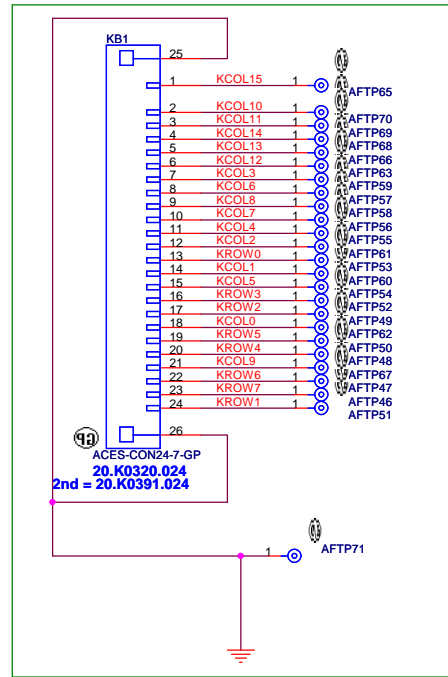
55.4KZ01.S18G S19G

緯創資通 Wistron Corporation
21F, 8F, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taiwan, R.O.C.

LED Bard/Power Button			
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SSID = KBC

Internal KeyBoard Connector

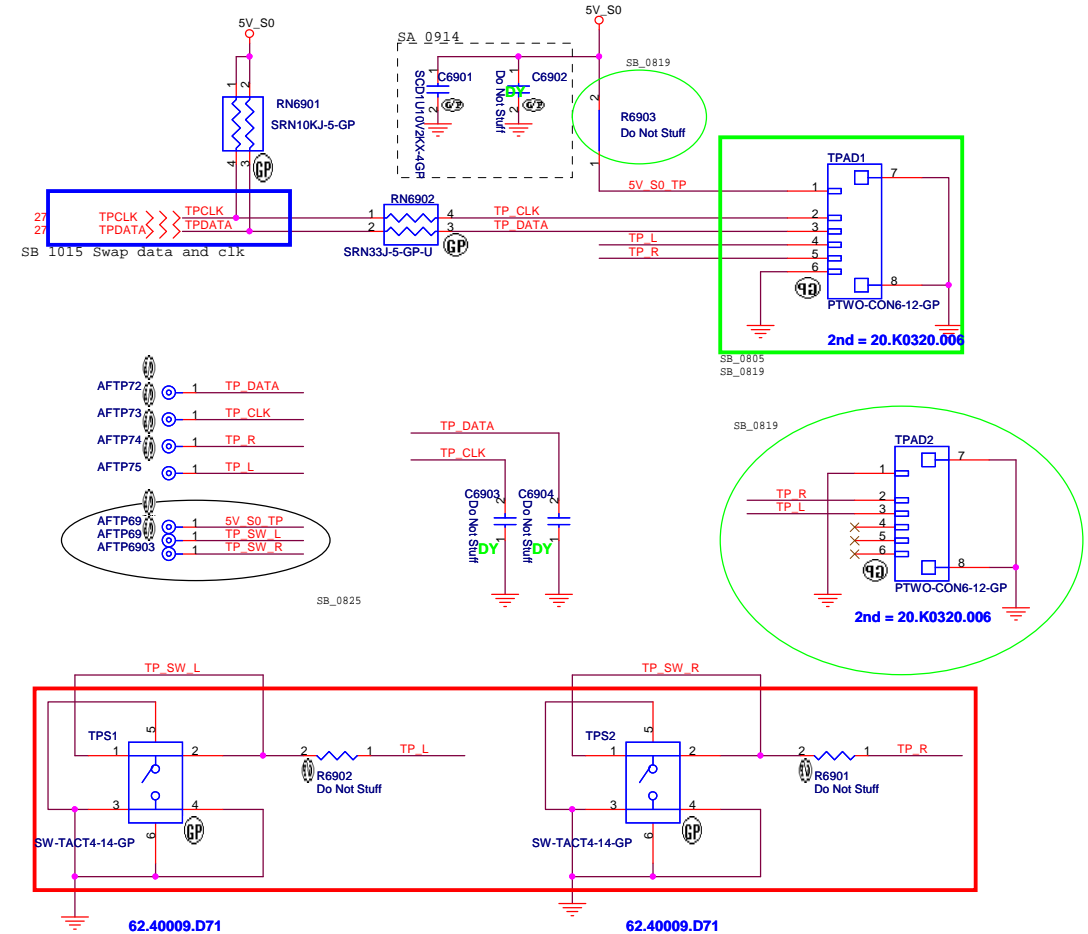


20100705

* Membrane Pin Out Top View :

PIN #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	12	1	8	9	5	6	3	2
As-sign	D 1	D 2	D 3	D 4	D 5	D 6	D 7	D 8	D 9	D 10	D 11	D 12	D 13	D 14	D 15	D 16	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8

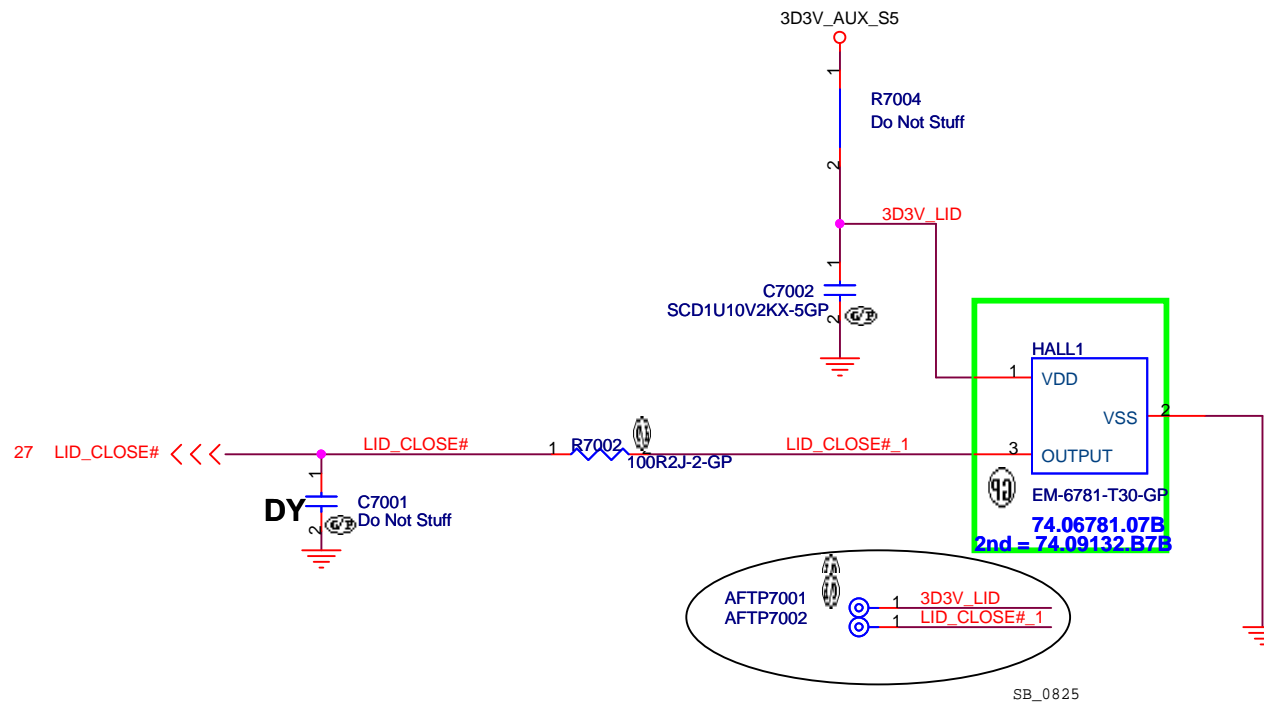
SSID = Touch.Pad



55.4KZ01.S18G S19G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			Key Board/Touch Pad
Size	Document Number	Rev	
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緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Hall Sensor

Size
A4

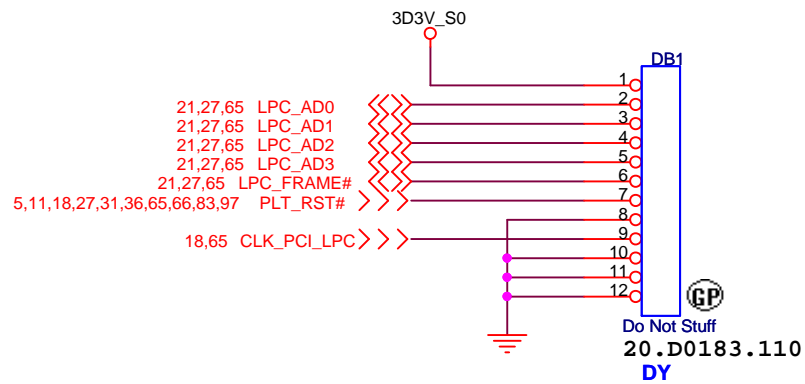
Document Number

LA470

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-1

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55.4KZ01.S18G S19G

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Dubug connector

Size
A4

Document Number

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-1

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55.4KZ01.S18G S19G

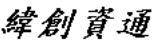
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<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>			
<div>Title</div>			
<div>Reserved</div>			
<div>Size</div>	<div>Document Number</div>	<div>Rev</div>	
<div>A3</div>	<div>LA470</div>	<div>-1</div>	
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55.4KZ01.S18G S19G

<div>緯創資通</div>		<div>Wistron Corporation</div>	
<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>			
<div>Title</div>			
<div>Reserved</div>			
<div>Size</div>	<div>Document Number</div>	<div>Rev</div>	
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5	4	3	2	1
D				
C				
B				
A				

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		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title				
CARD Reader CONN				
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	5	4	3	2	1
D					
C					
B					
A					

55.4KZ01.S18G S19G

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
New Card			
Size A3	Document Number LA470		Rev -1
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55.4KZ01.S18G S19G

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>LA470</div>	Rev <div>-1</div>
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55.4KZ01.S18G S19G

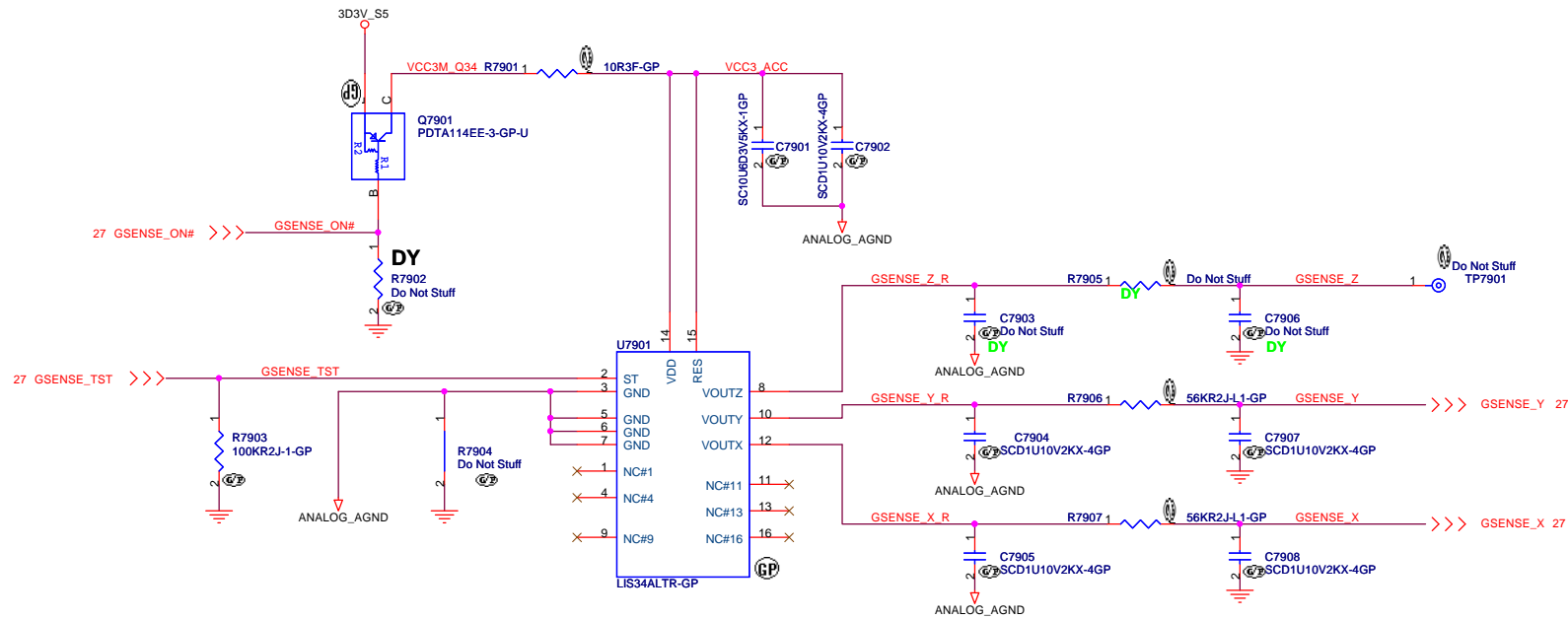
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TitleReserved		
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55.4KZ01.S18G S19G

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
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Size <div>A4</div>	Document Number <div>LA470</div>	Rev <div>-1</div>
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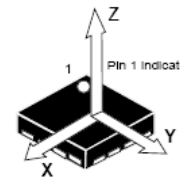
G-Sensor



STMicro LIS34AL: 74.00034.0BZ
ADXL335 : 74.00335.0BZ

Layout Comment :

- (1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.
- (2) Avoid routing under DCDC switching area.



	ADXL322	
	LIS244AL	No Accel
	LIS34AL	
R530	NO_ASM	ASM
R509	ASM	ASM
All other	ASM	NO_ASM

55.4KZ01.S18G S19G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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55.4KZ01.S18G S19G

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>LA470</div>	Rev <div>-1</div>
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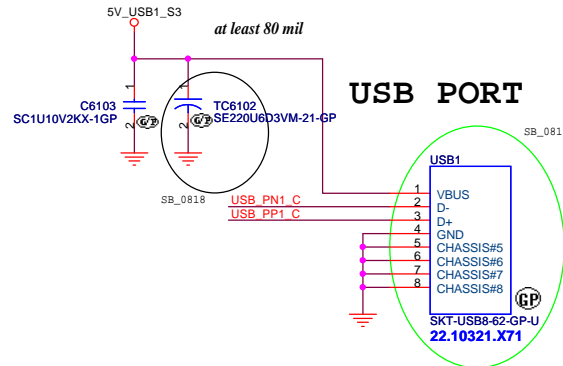
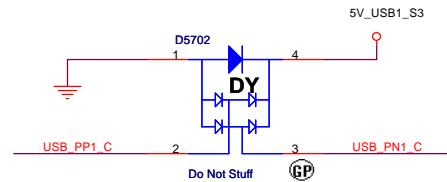
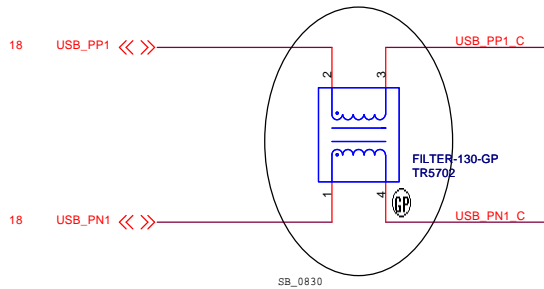
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55.4KZ01.S18G S19G

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>LA470</div>	Rev <div>-1</div>
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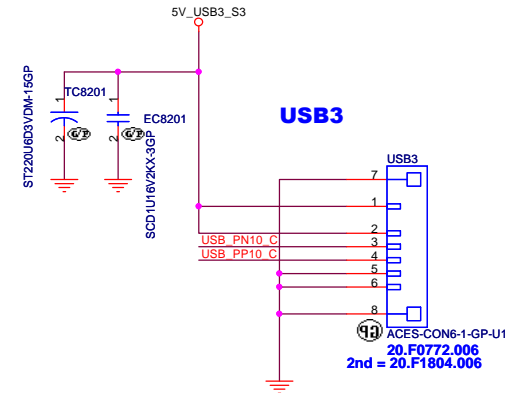
IO Board CONN 80 pin

USB1

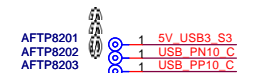
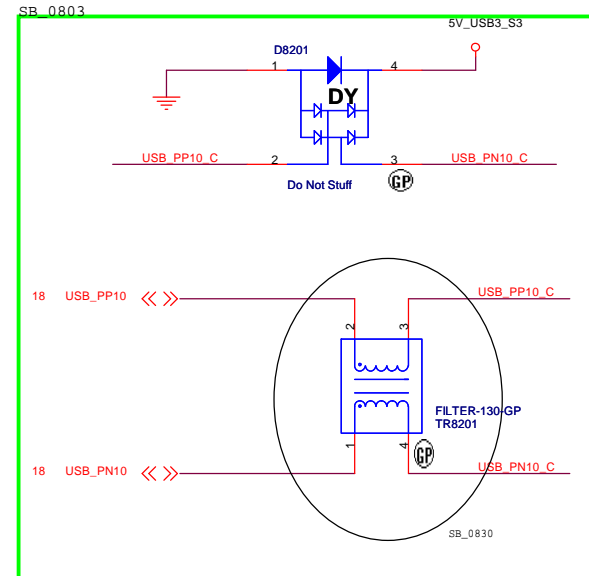
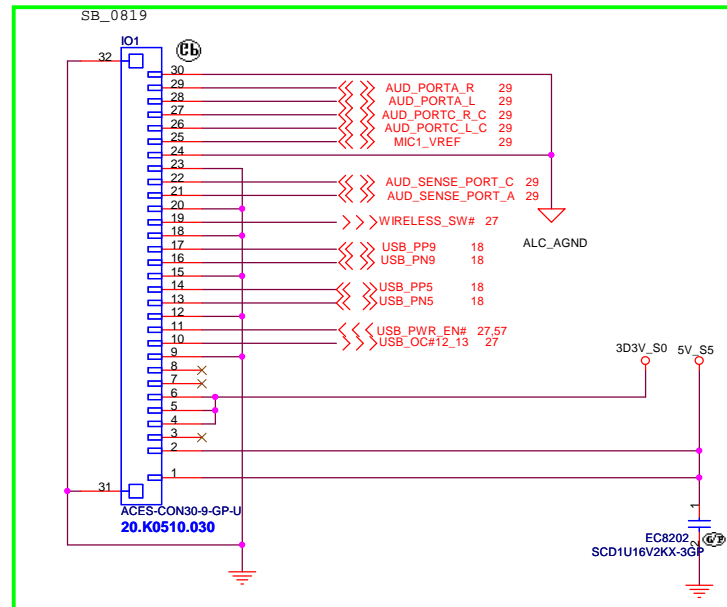
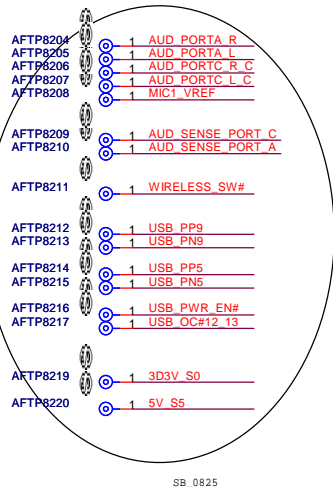


Mars:
Exchange ODD and ESATA differential pair each other.

USB Board CONN.



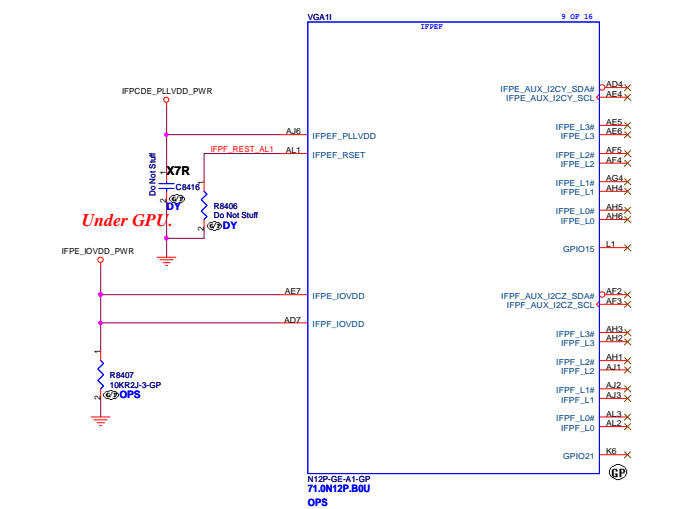
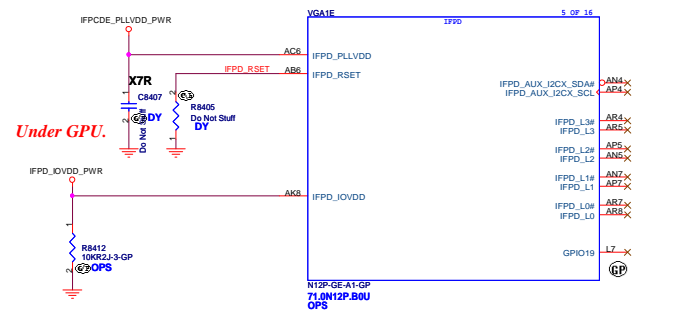
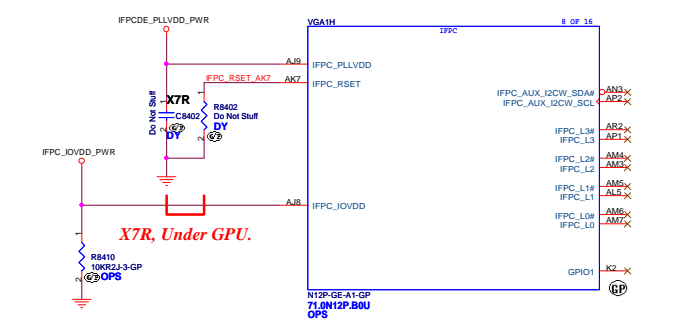
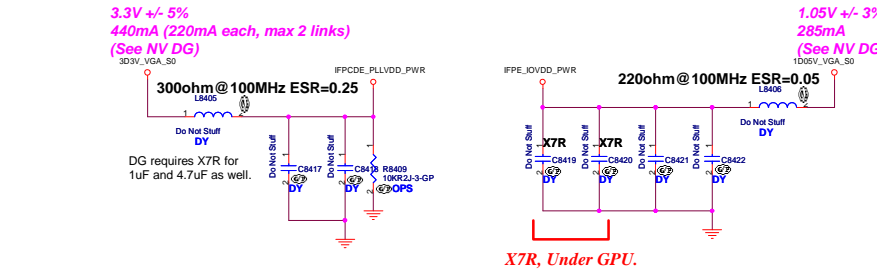
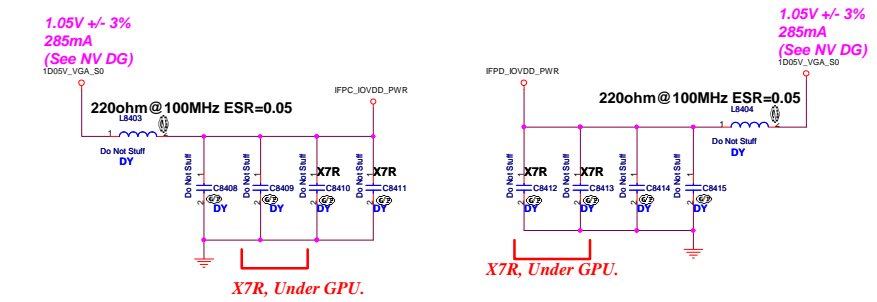
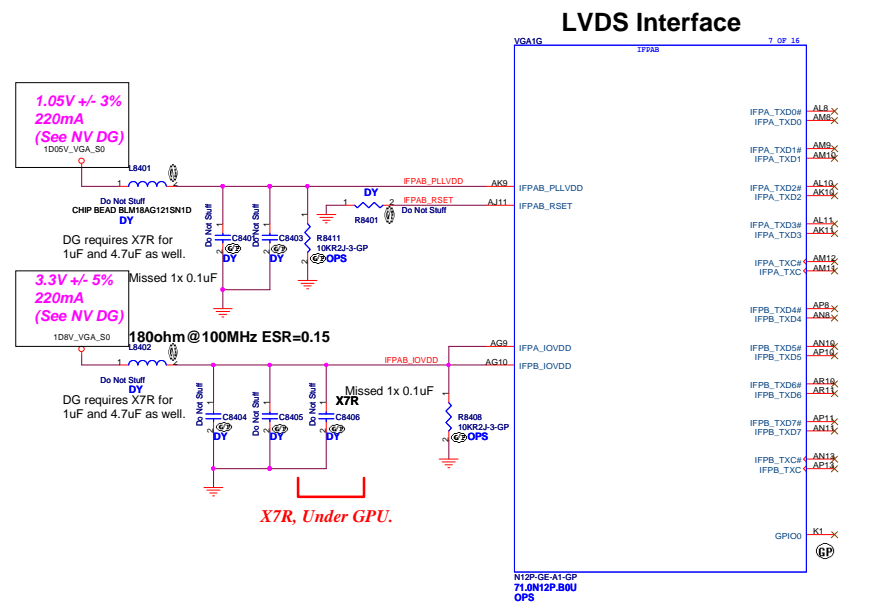
I/O Board CONN.



55.4K201.S18G S19G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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IO Board Connector		
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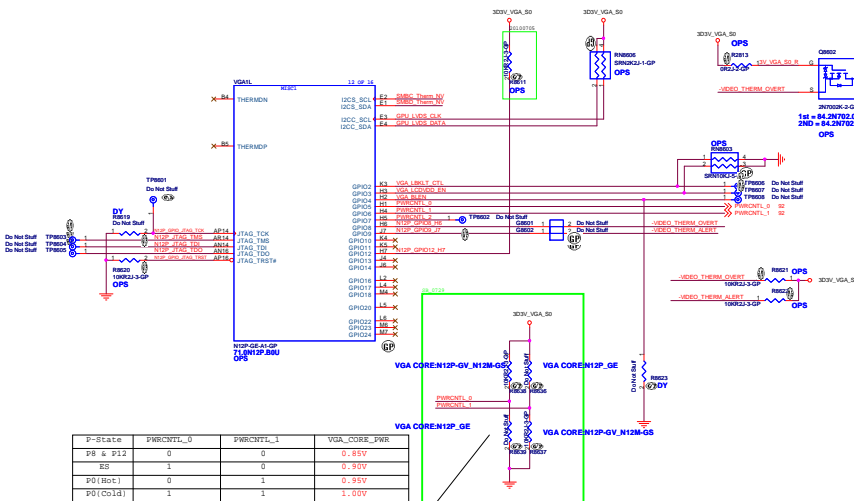
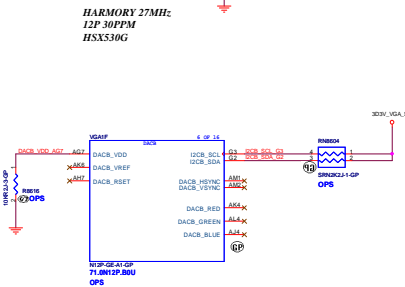
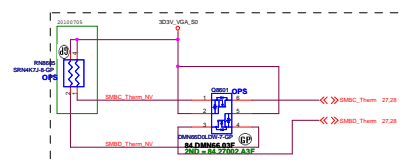
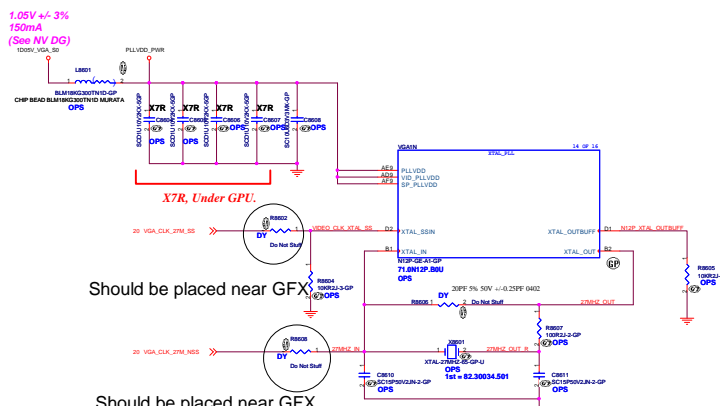
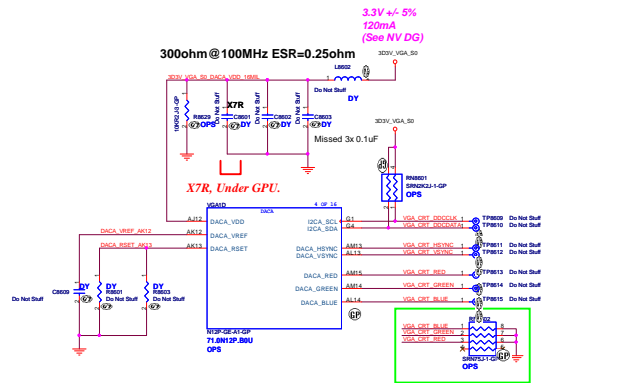
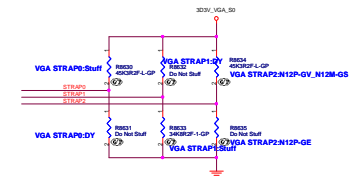


TABLE
VIDEO MEMORY

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800MHz	72.52G63.00U	72.42164.C0U	72.51G63.C0U	72.41164.H0U
ROM_SI	34.8Kohm	45.3Kohm	15Kohm	20Kohm
PD R8627	64.34825.6DL	64.45325.6DL	64.15025.6DL	64.20025.6DL

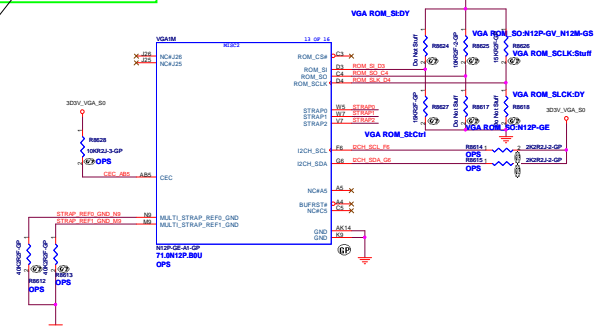


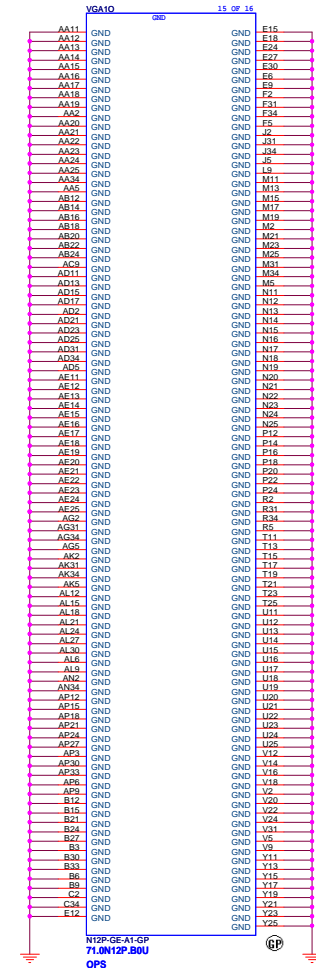
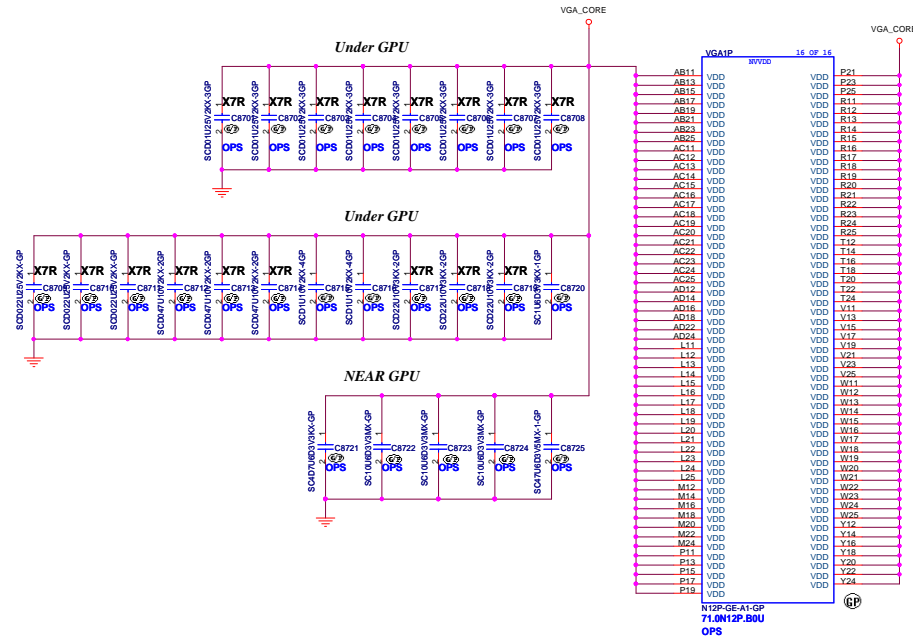
P-State	PWRCTRL_0	PWRCTRL_1	VGA_CORE_PWR
P8 & P12	0	0	0.95V
P8	1	0	0.90V
P0(Not)	0	1	0.95V
P0(CoD)	1	1	1.00V

P-State	N12P-GE	N12P-GV1	N12M-GE	N12P-GV
W7V00 Boot Voltage	0.95V	0.90V	0.85V	0.90V
R8636	StuF	DY	DY	DY
R8637	DY	StuF	StuF	StuF
R8638	DY	StuF	DY	StuF
R8639	StuF	DY	StuF	DY

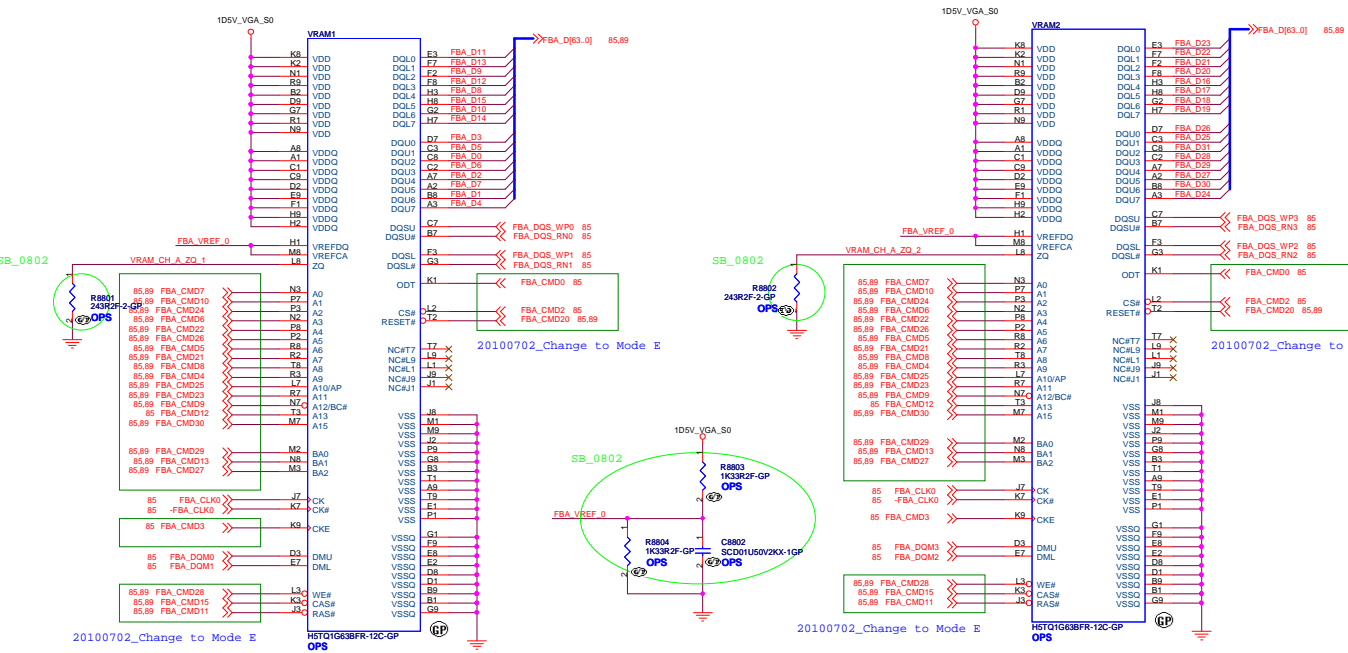
LOGIC

TABLE NVIDIA	N12P-GE DEV ID: 0x0DF5 0101	N12P-GV DEV ID: 0x0DF7(ES)	N12M-GE DEV ID: 0xA7A 1010
STRAP1	R8632 DY	DY	35Kohm 64.34825.6DL
	R8633 35Kohm 64.34825.6DL	35Kohm 64.34825.6DL	DY
STRAP2	R8634 DY	45Kohm 64.45325.6DL	15Kohm 64.15025.6DL
	R8635 30Kohm 64.30025.6DL	DY	DY

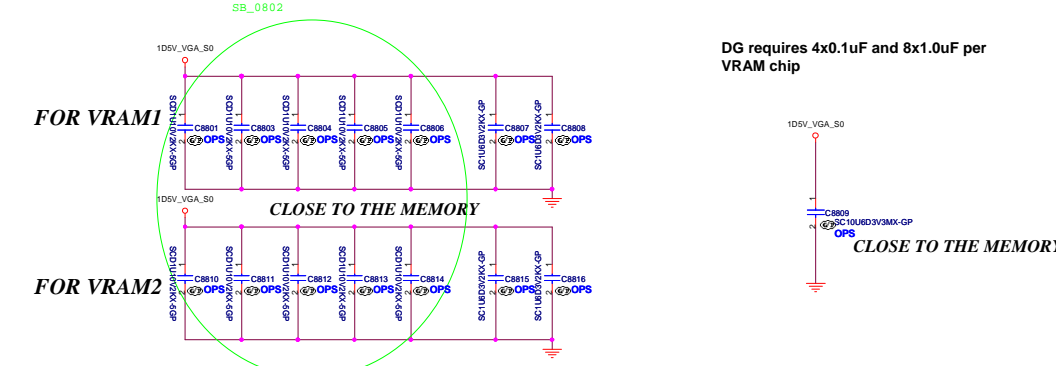




55.KZ01.S18G S19G



FB CMD mapping Mode D-N12x



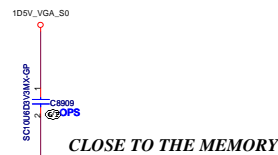
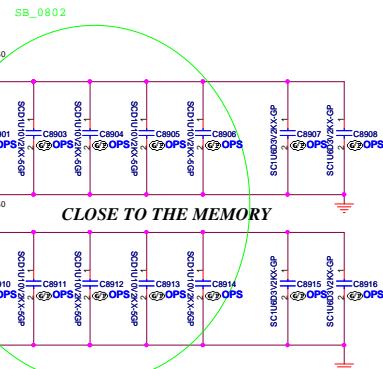
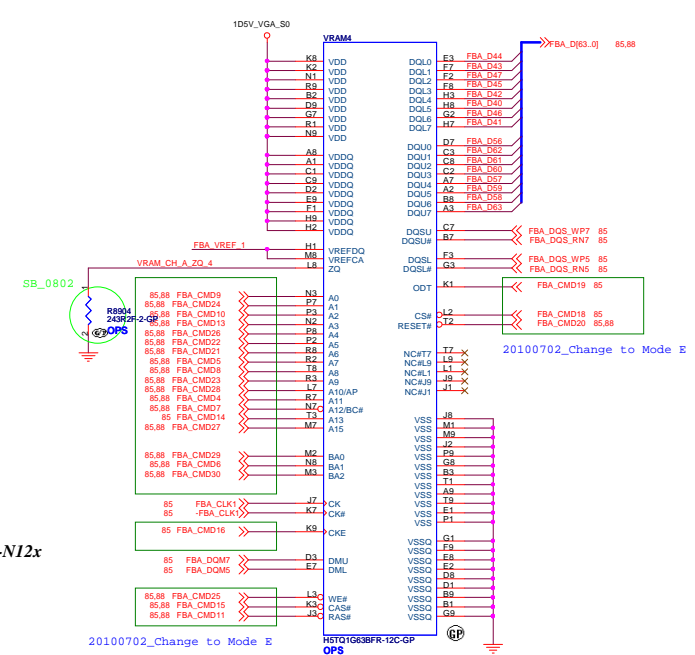
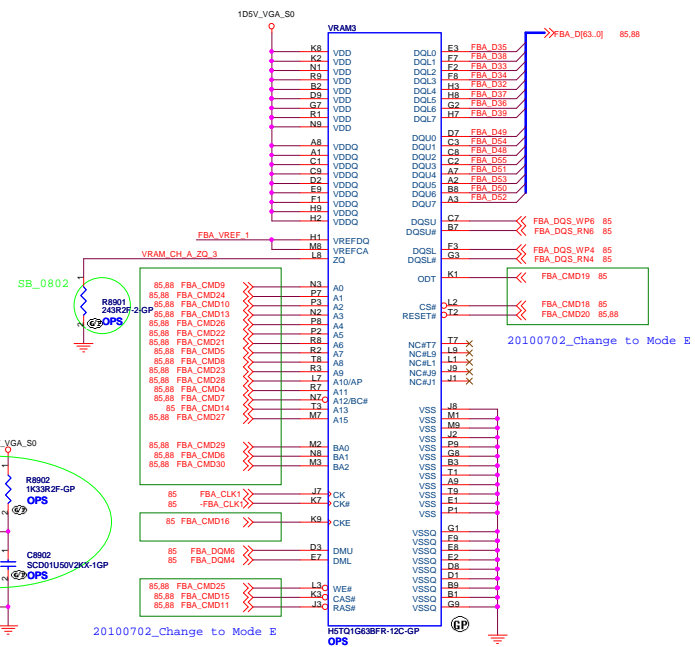
DG requires 4x0.1uF and 8x1.0uF per VRAM chip



VIDEO FRAME BUFFER PORT A

55.4KZ01.S18G S19G	
緯創資通 Wistron Corporation	
21F, 8B, Sec. 1, Hsin Tai Wu Rd., Hsueh, Taipei Hsien 221, Taiwan, R.O.C.	
Title VRAM CHANNEL-A	
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FB CMD mapping Mode D-N12x

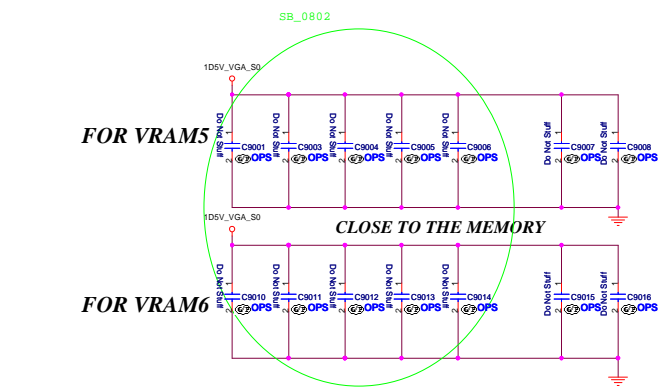
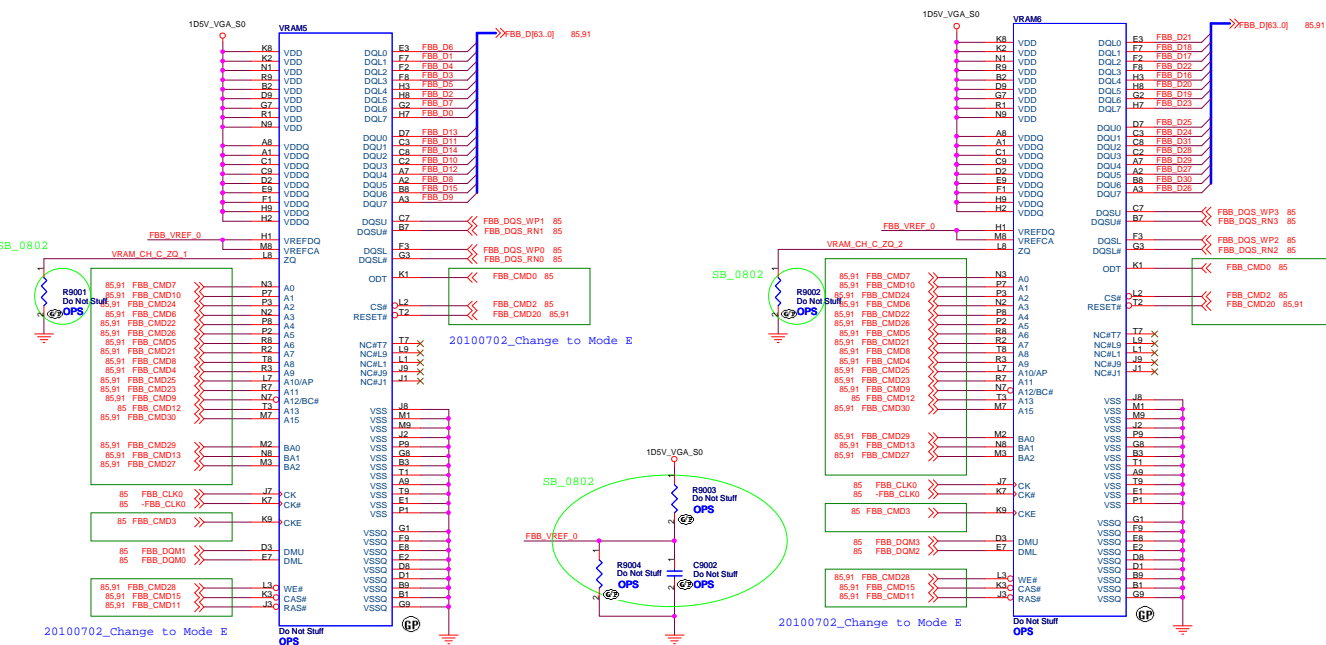


VIDEO FRAME BUFFER PORT A

55.4KZ01.S18G S18G

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsuehshui, Taipei Hsien 221, Taiwan, R.O.C.

Title		
VRAM CHANNEL-A		
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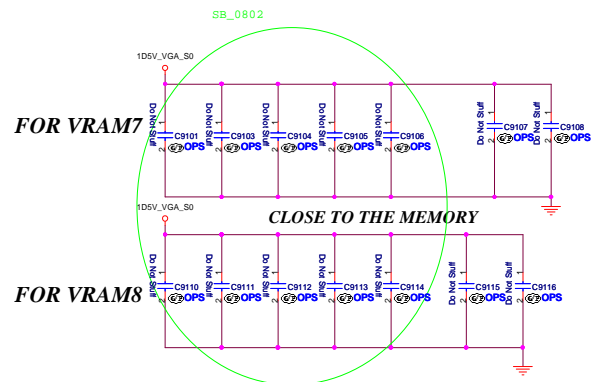
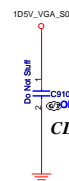
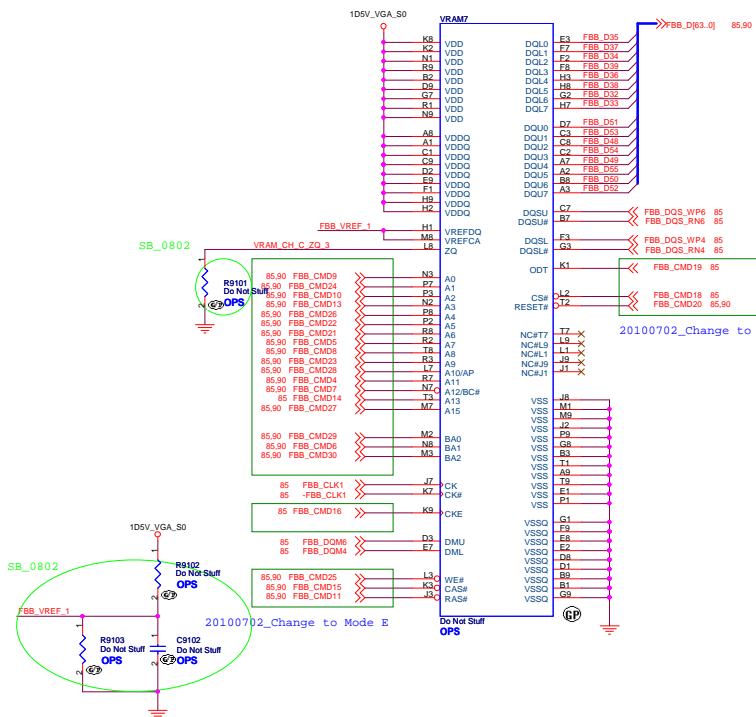


DG requires 4x0.1uF and 8x1.0uF per VRAM chip

CLOSE TO THE MEMORY

VIDEO FRAME BUFFER PORT C

55.4KZ01.S18G S19G			
緯創資通 Wistron Corporation			
21F, 8B, Sec. 1, Hsin Tai Wu Rd., Hsuehshui, Taipei Hsien 221, Taiwan, R.O.C.			
Title VRAM CHANNEL-C			
Size A2	Document Number LA470	Rev -1	
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VIDEO FRAME BUFFER PORT C

55.4KZ01.S18G S19G

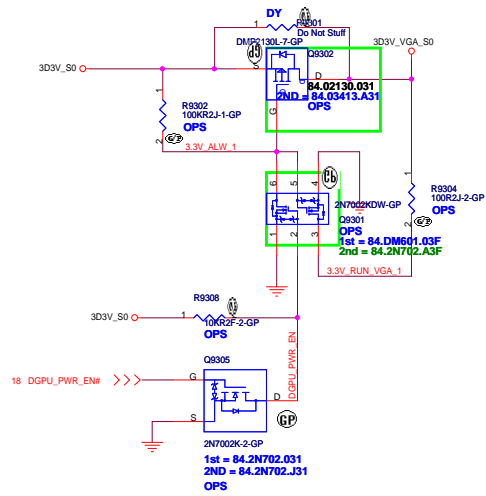
緯創資通 Wistron Corporation
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsueh,
Taipei Hsien 221, Taiwan, R.O.C.

Title VRAM CHANNEL-C

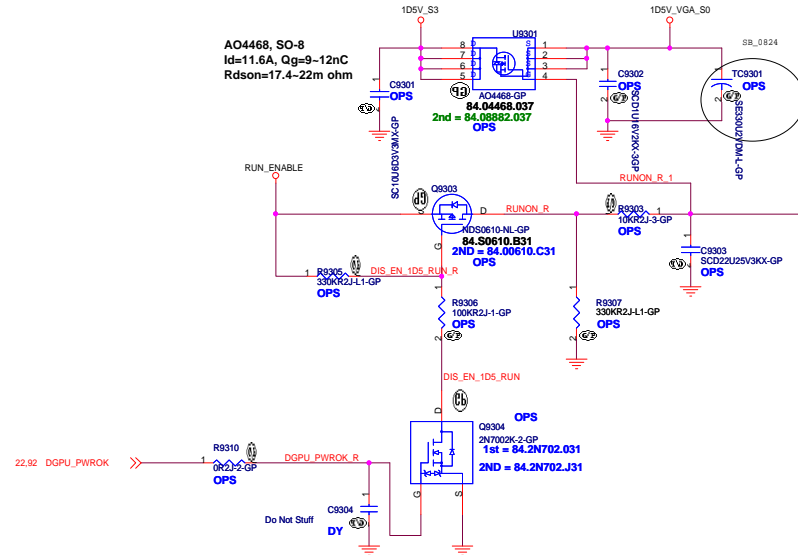
Size A2 Document Number LA470 Rev -1

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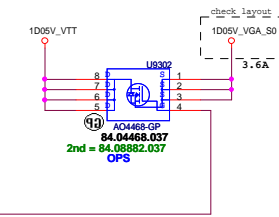
+3VS to 3.3V_DELAY Transfer



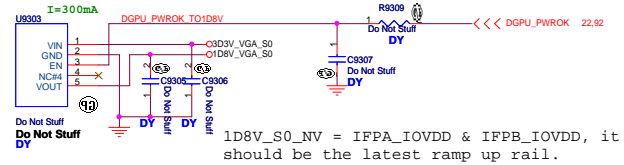
1D5V_VGA_S0



1.05V to 1.05V_VGA_S0 Transfer



+3VS to 1.8V Transfer



55.4K201.S18G S19G

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Title DISCRETE VGA POWER		
Size	Document Number LA470	Rev -1
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55.4KZ01.S18G S19G

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Title			
CRT Switch			
Size	Document Number		Rev
A3	LA470		-1
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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
TOUCH PANEL		
Size	Document Number	Rev
A4	LA470	-1
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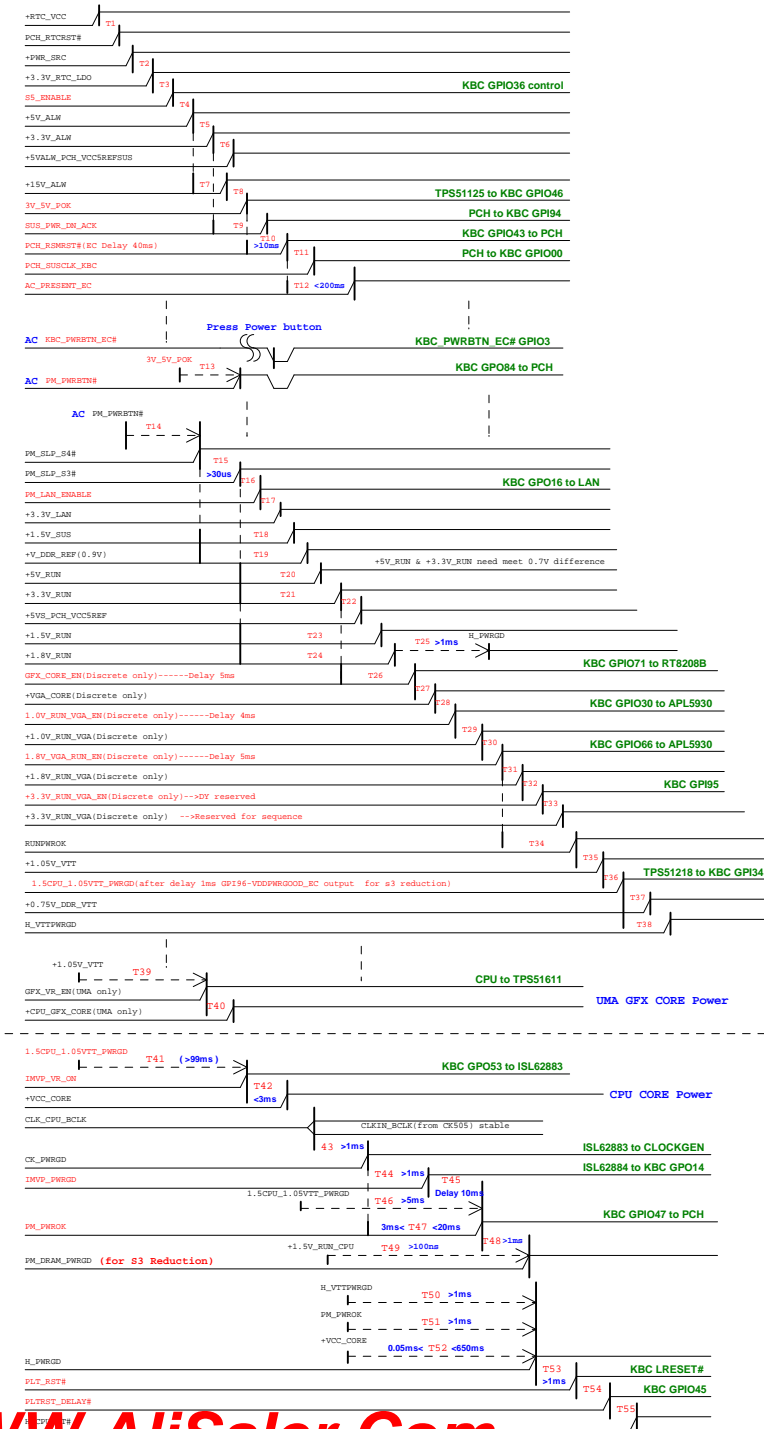
55.4KZ01.S18G S19G

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>Change History</i>			
Size A4	Document Number LA470		Rev -1
Date:	Thursday, November 04, 2010	Sheet 98 of	103

Intel-Power Up Sequence

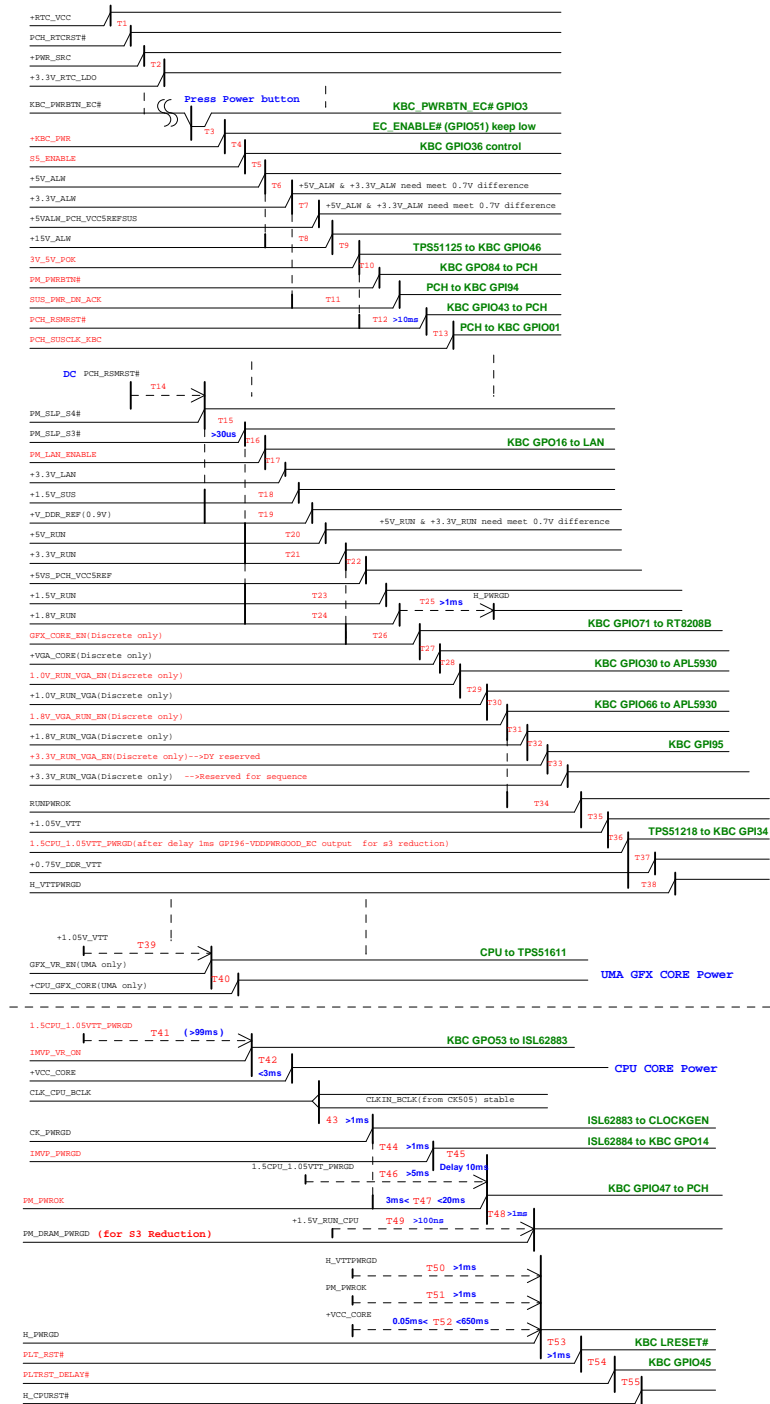
(AC mode)

red word: KBC GPIO



(DC mode)

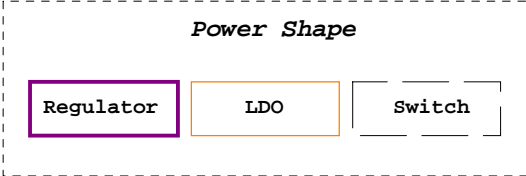
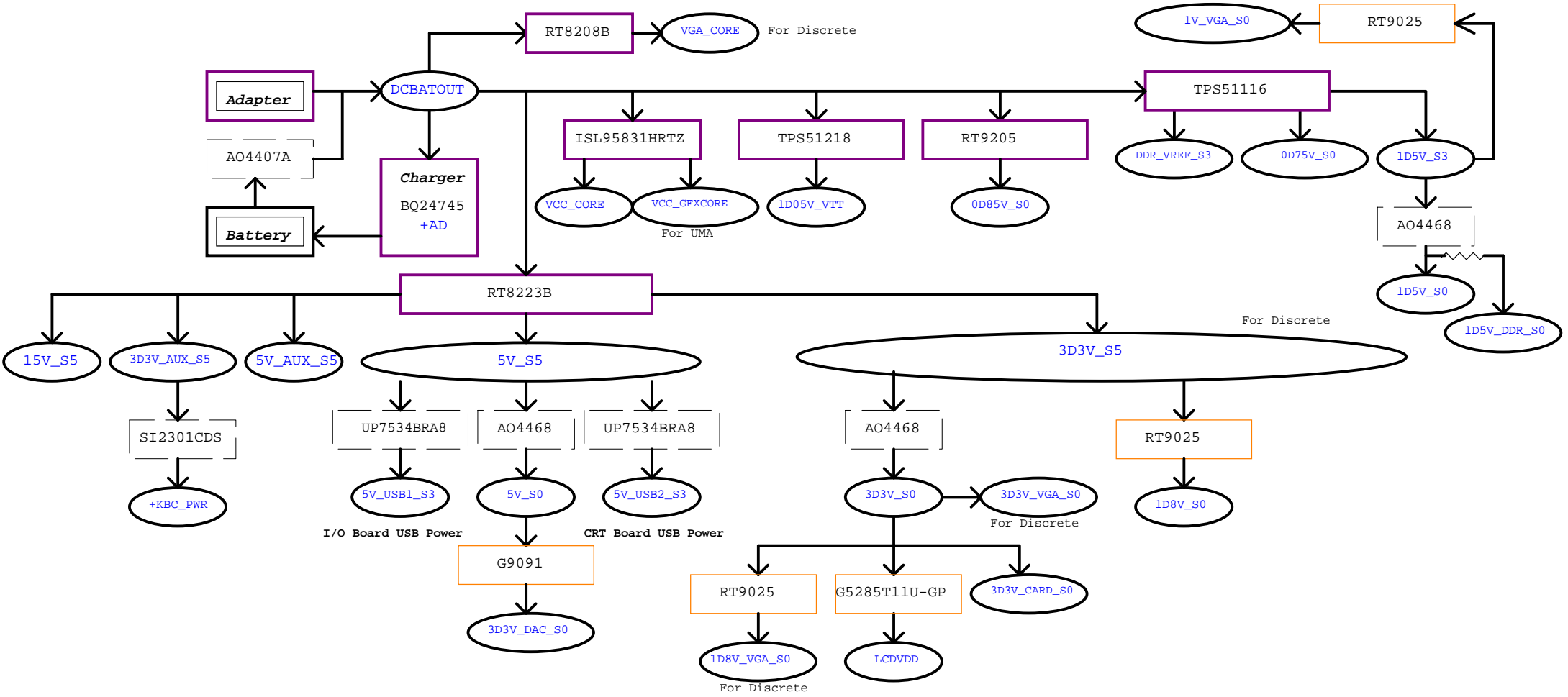
red word: KBC GPIO



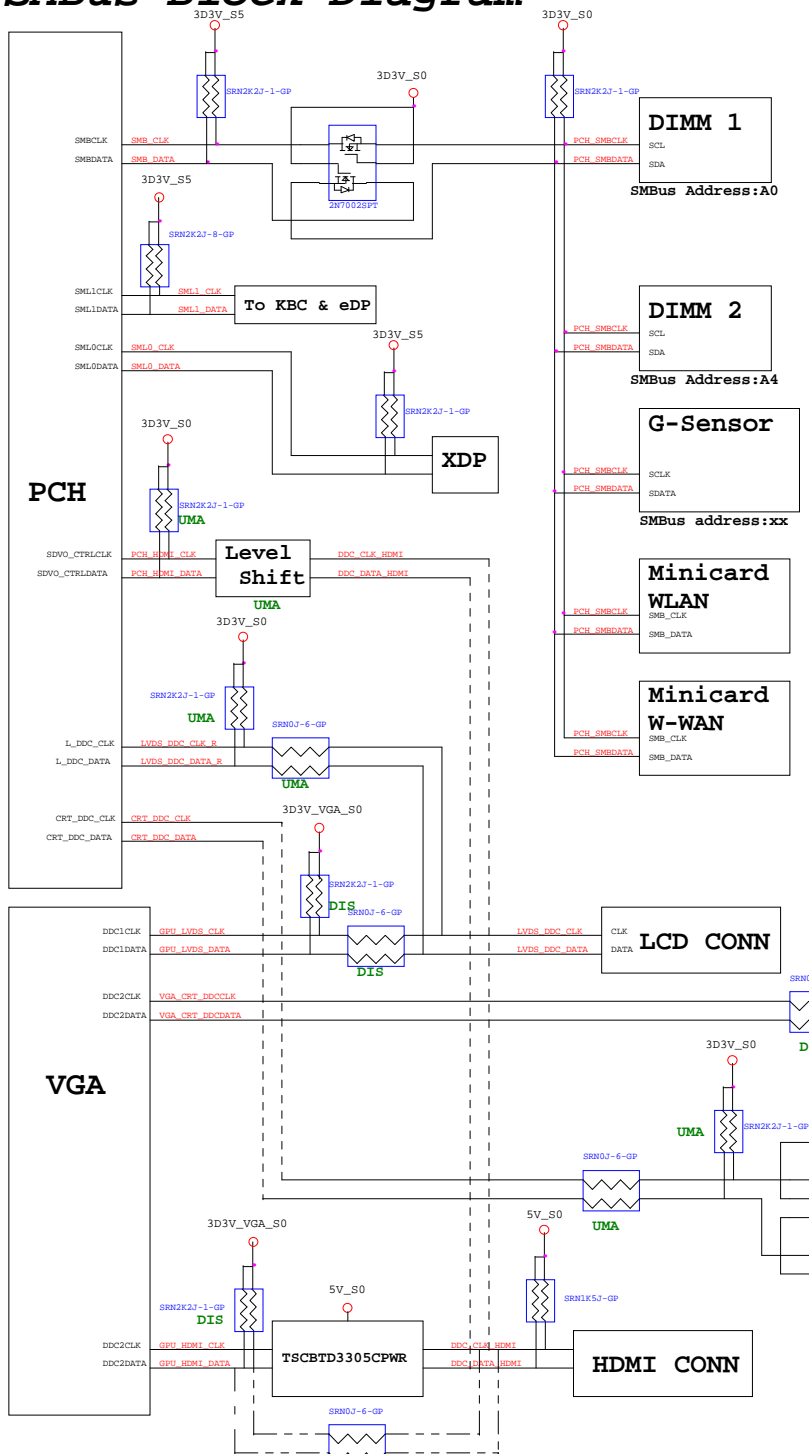
SL46201, 51845, 51940

Wistron Corporation
33F, 38, Sec. 2, Hsin-Fu Rd., Hsinchu, Taiwan, R.O.C.

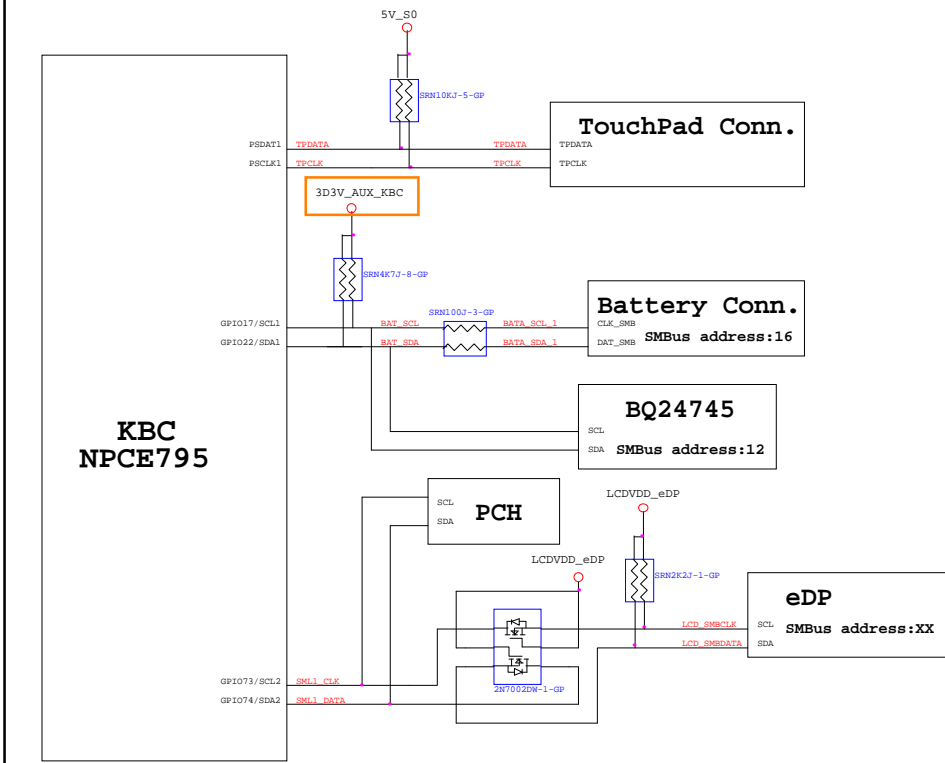
Power Sequence
LA470
-1



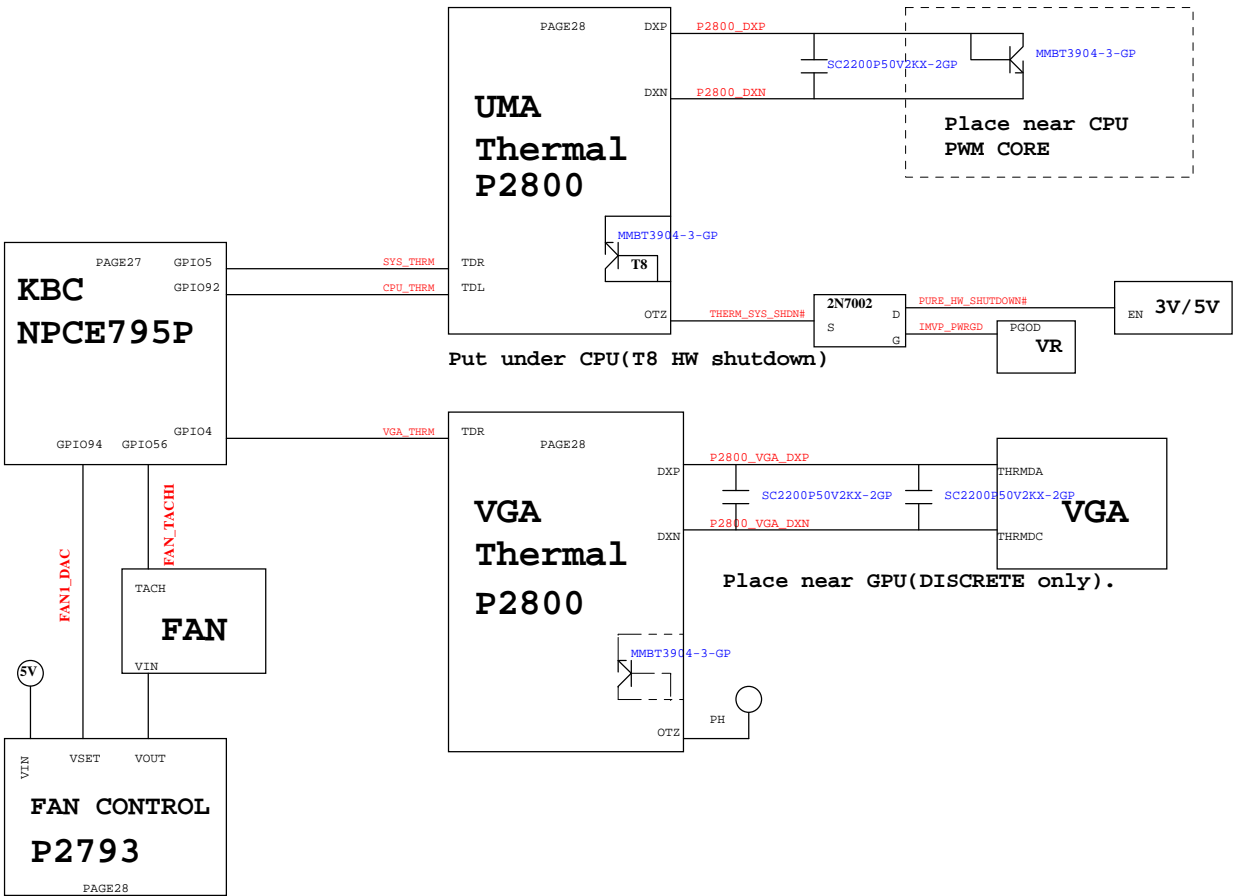
PCH SMBus Block Diagram



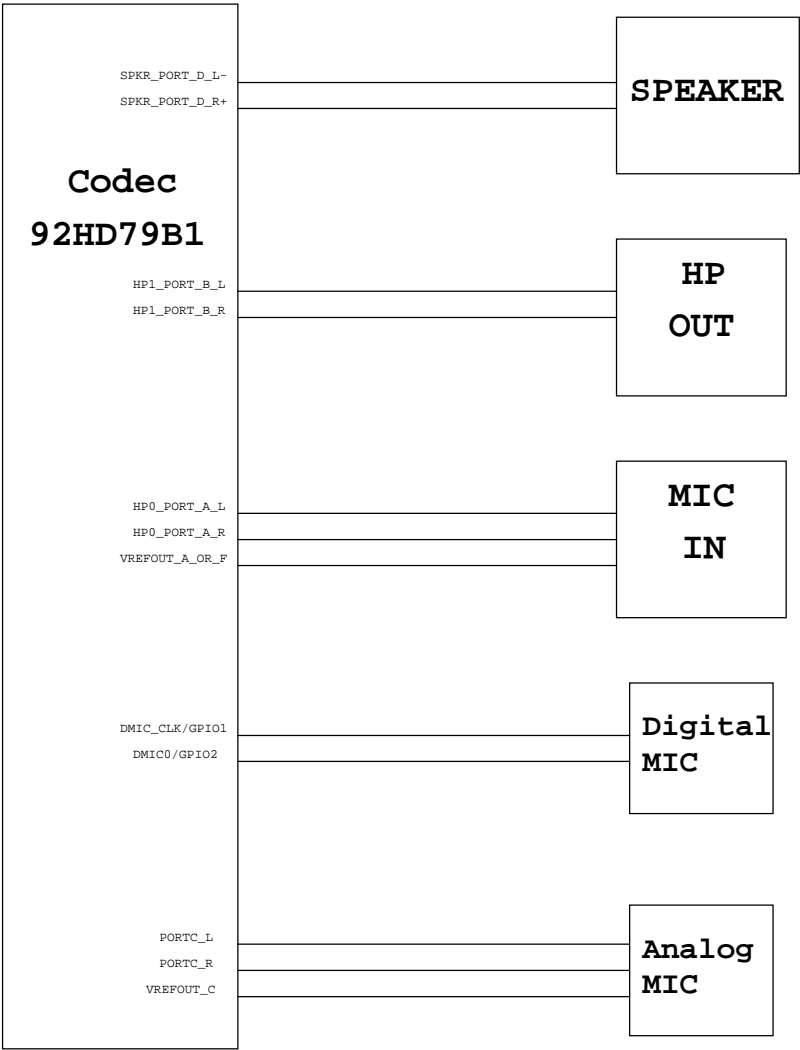
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



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Title		
Change History		
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